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P. Leader	Check by	Design by

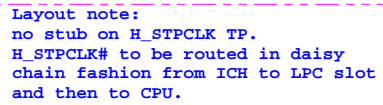
Project Code & Schematics Subject: M610 PVT Main Board

PCB P/N: 黃田 1P-0072100-8010
翰宇博德 1P-0072500-8010FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

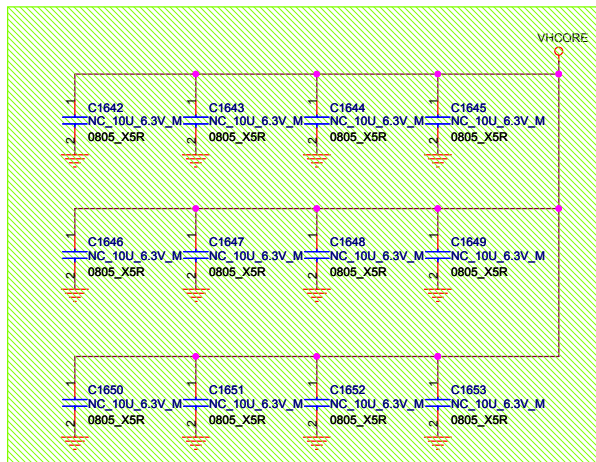
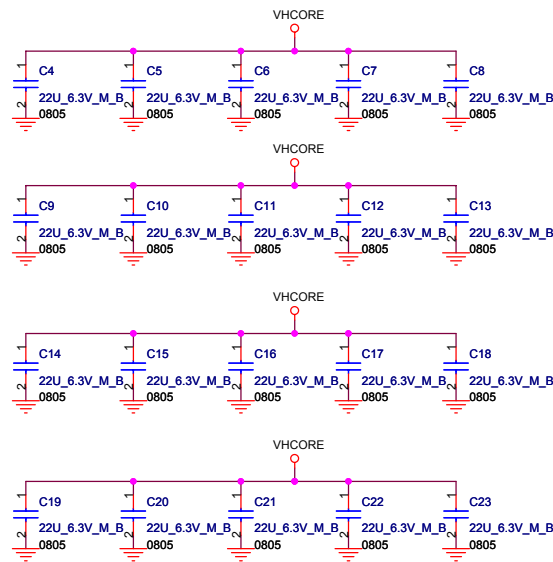
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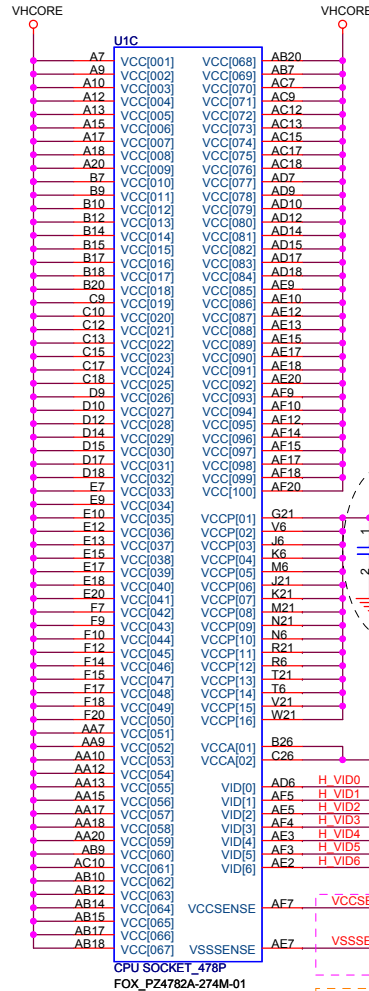
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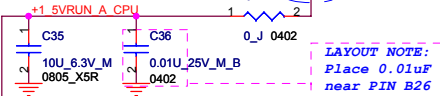
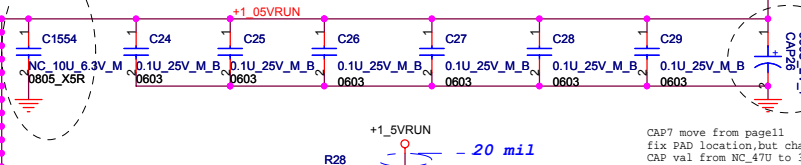
CPU_VCCA----->130mA
CPU_VCCP----->4.5A
CPU_VCC----->44A



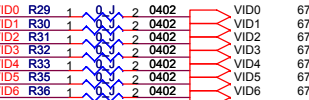
Backup 10uF capacitors for 22uF shortage.



Beagle1=10U
CRB1.301=NO
2H5C=1.201=NO
MS90 5V1=NO



LAYOUT NOTE:
Place 0.01uF
near PIN B26



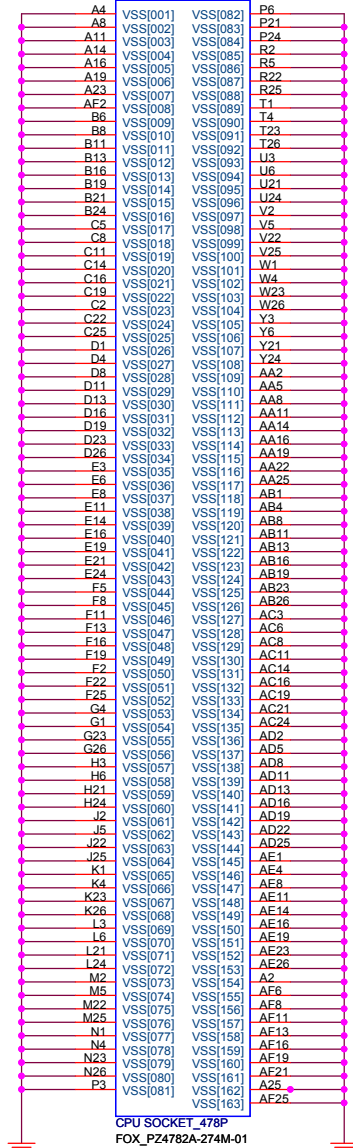
Layout Note: Route
VCCSENSE traces at 27.4
Ohms with 50 mil spacing.
Place PU and PD within 1
inch of cpu.

width=18 mil
spacing=7 mil

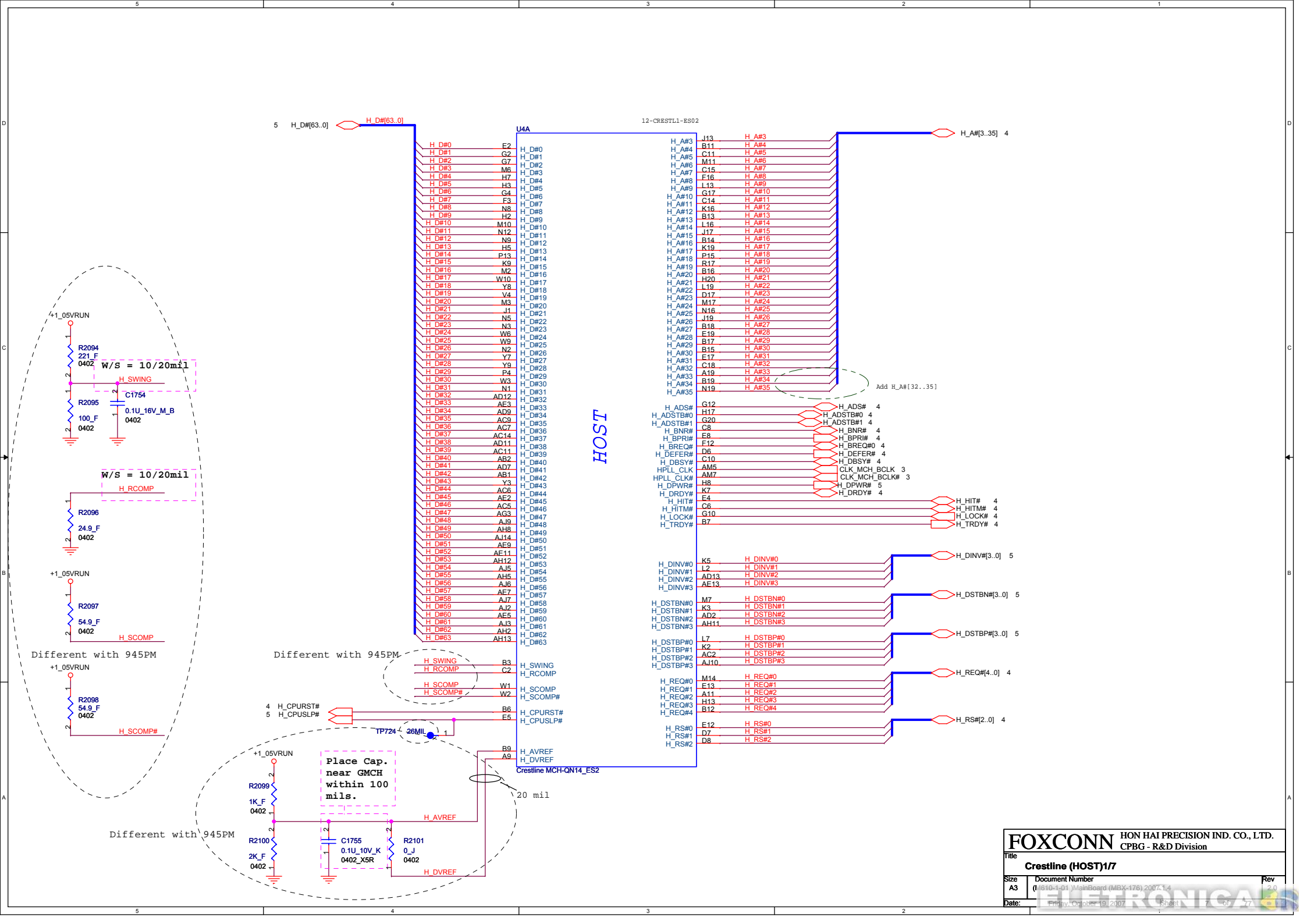
(Design check 1.301) 2006.9.3
No Stuff 27.4 ± 1% pull-down to GND
near Intel MVP 6 controller for testing purposes.

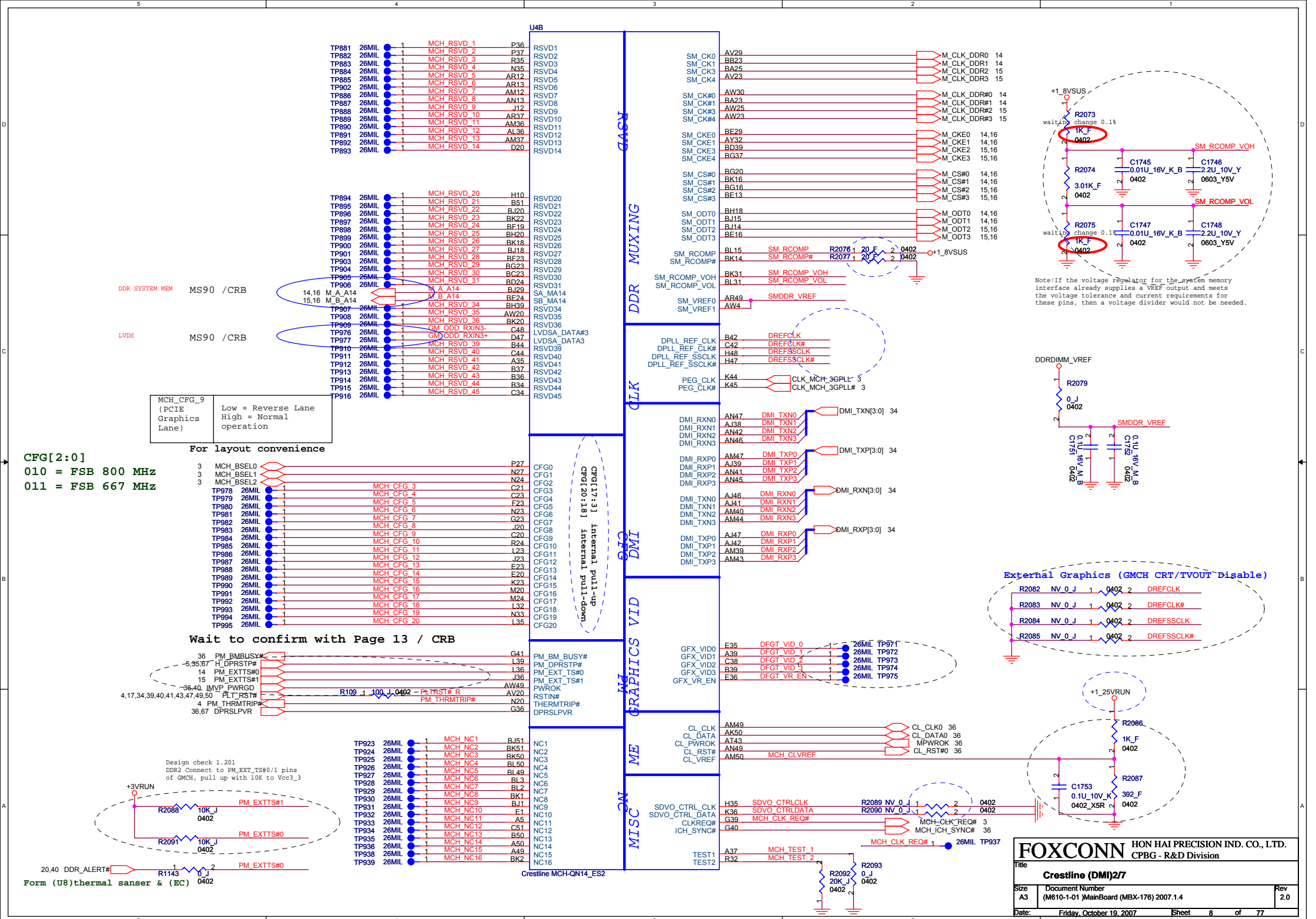
MS90 check

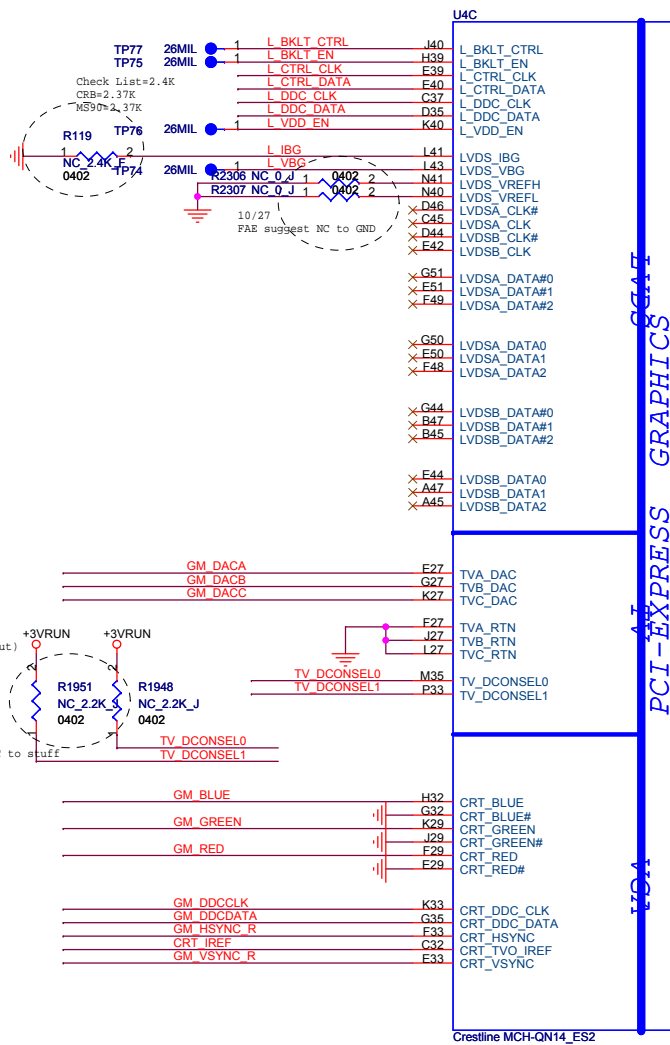
U1D



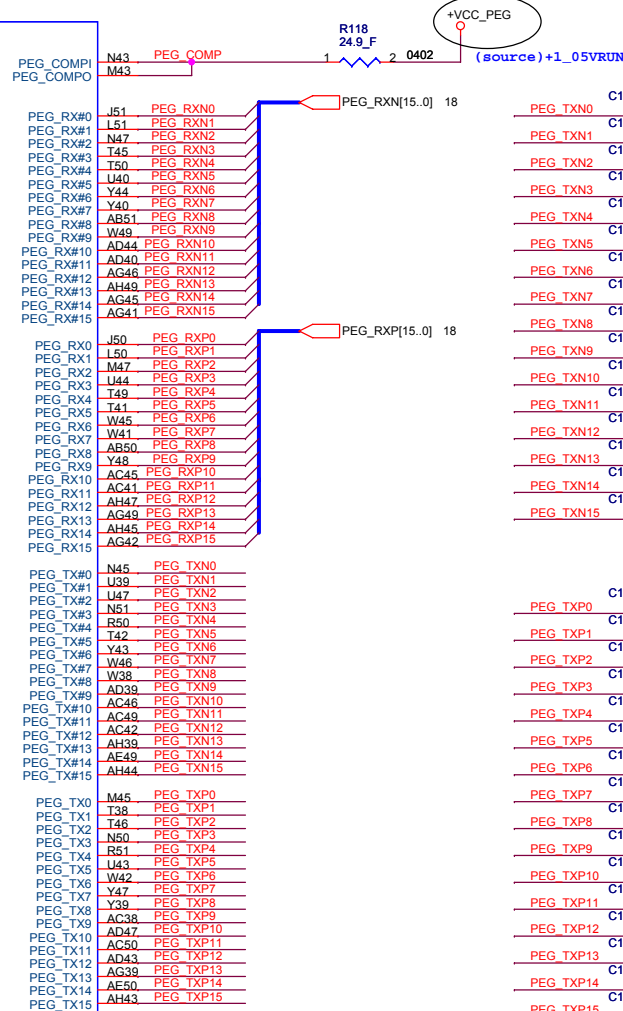
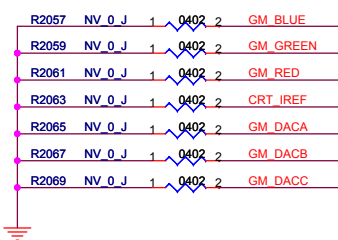
CPU SOCKET_478P
FOX_P24782A-274M-01







External Graphics (GMCH CRT/TVOUT Disable)



Base on below document:

Mobile Merom Processor and Crestline Chipset
- Santa Rosa Platform Design Guide-21112.1.0
.pvd.pdf (May 2006/ Rev 1.0)page 193

Table 82. External Graphics (GMCH Integrated Graphics Disable)
Connect these signals to GND

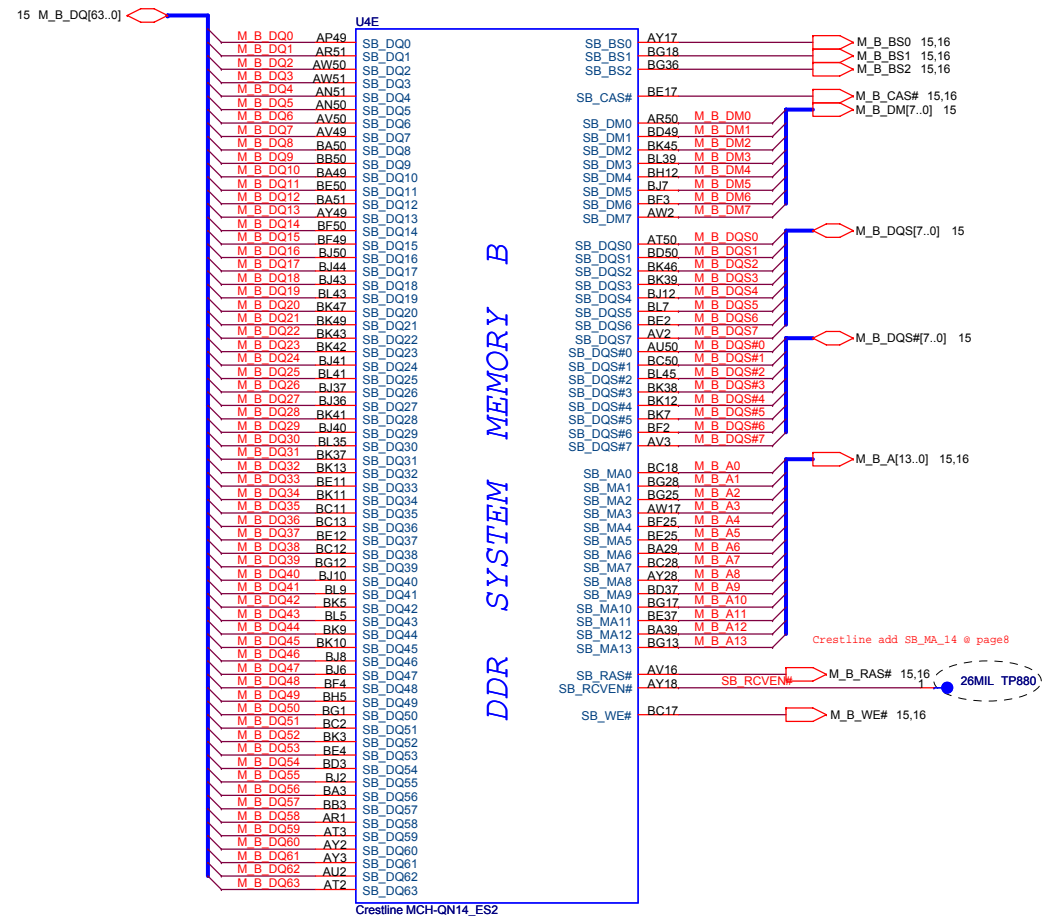
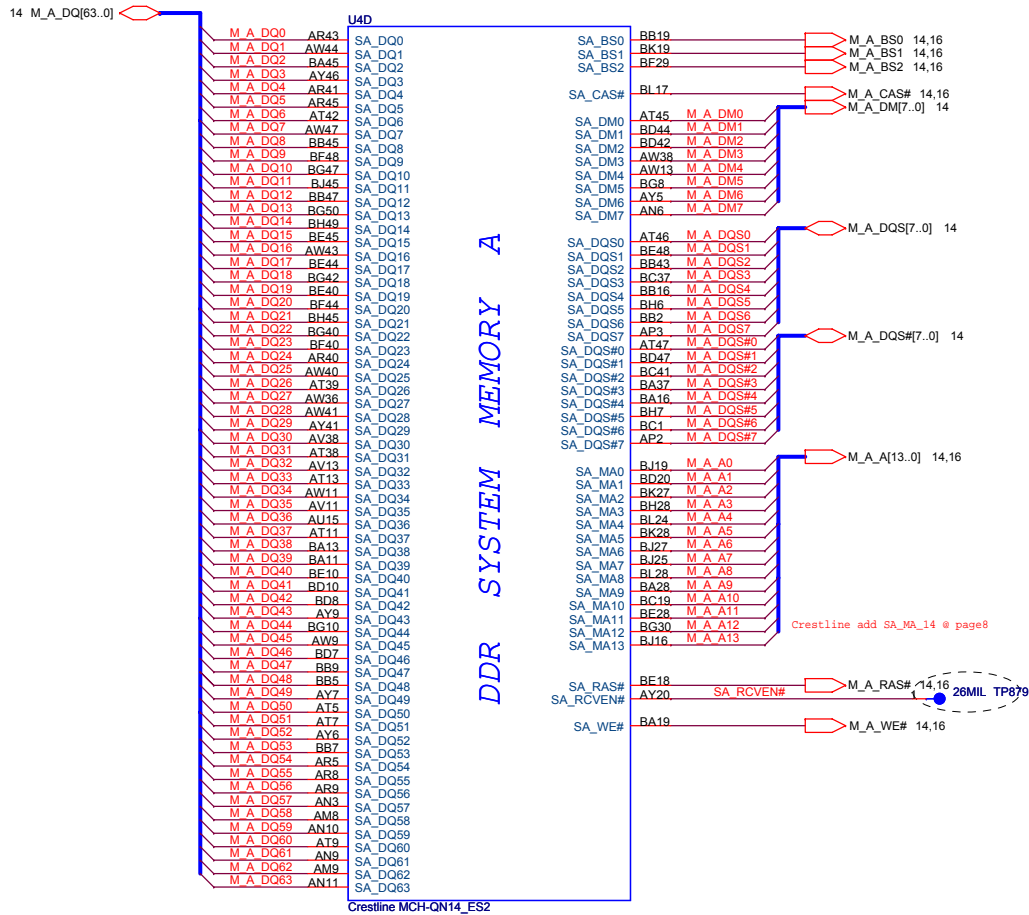
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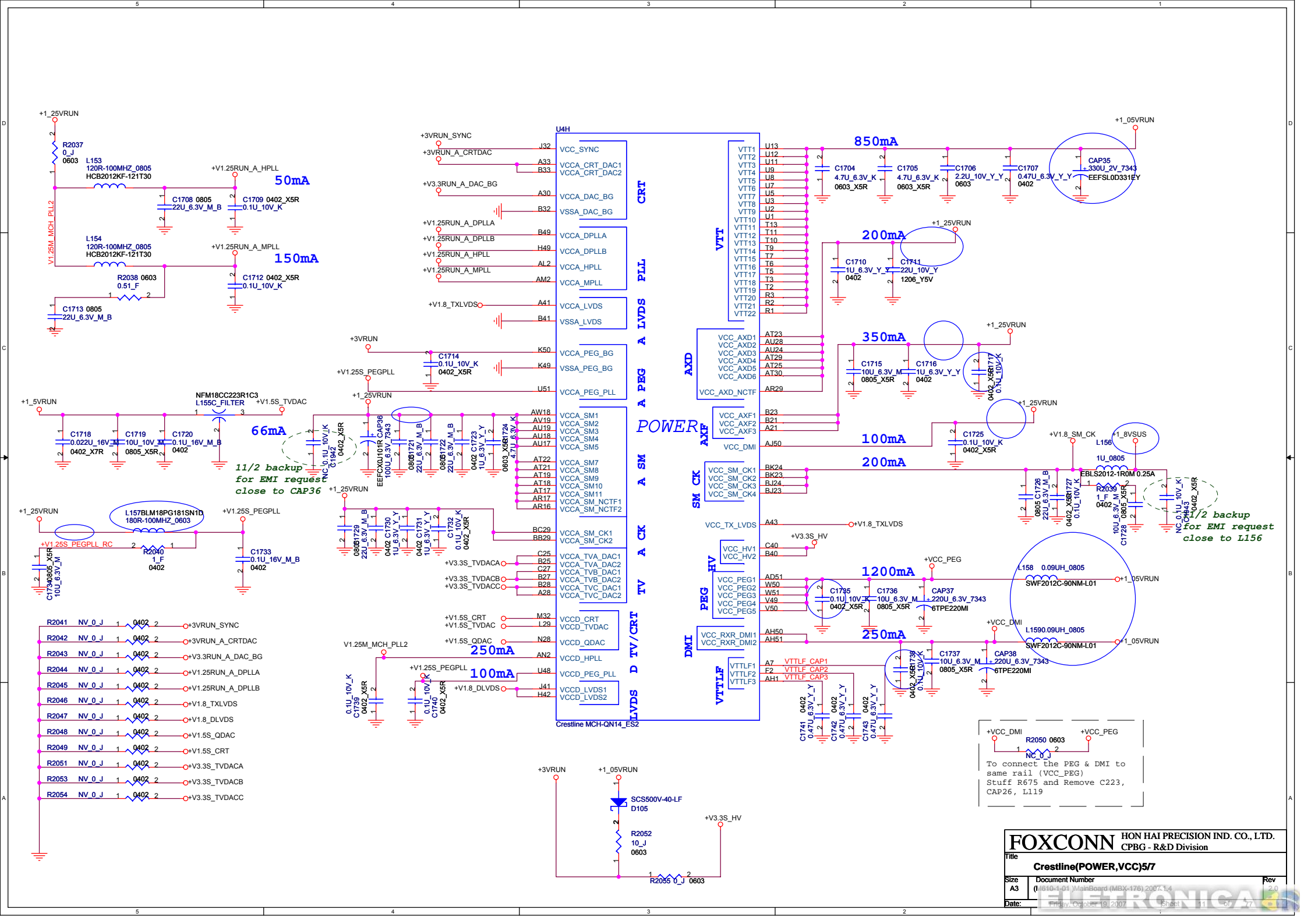
Title
Crestline(GRAPHIC)3/7

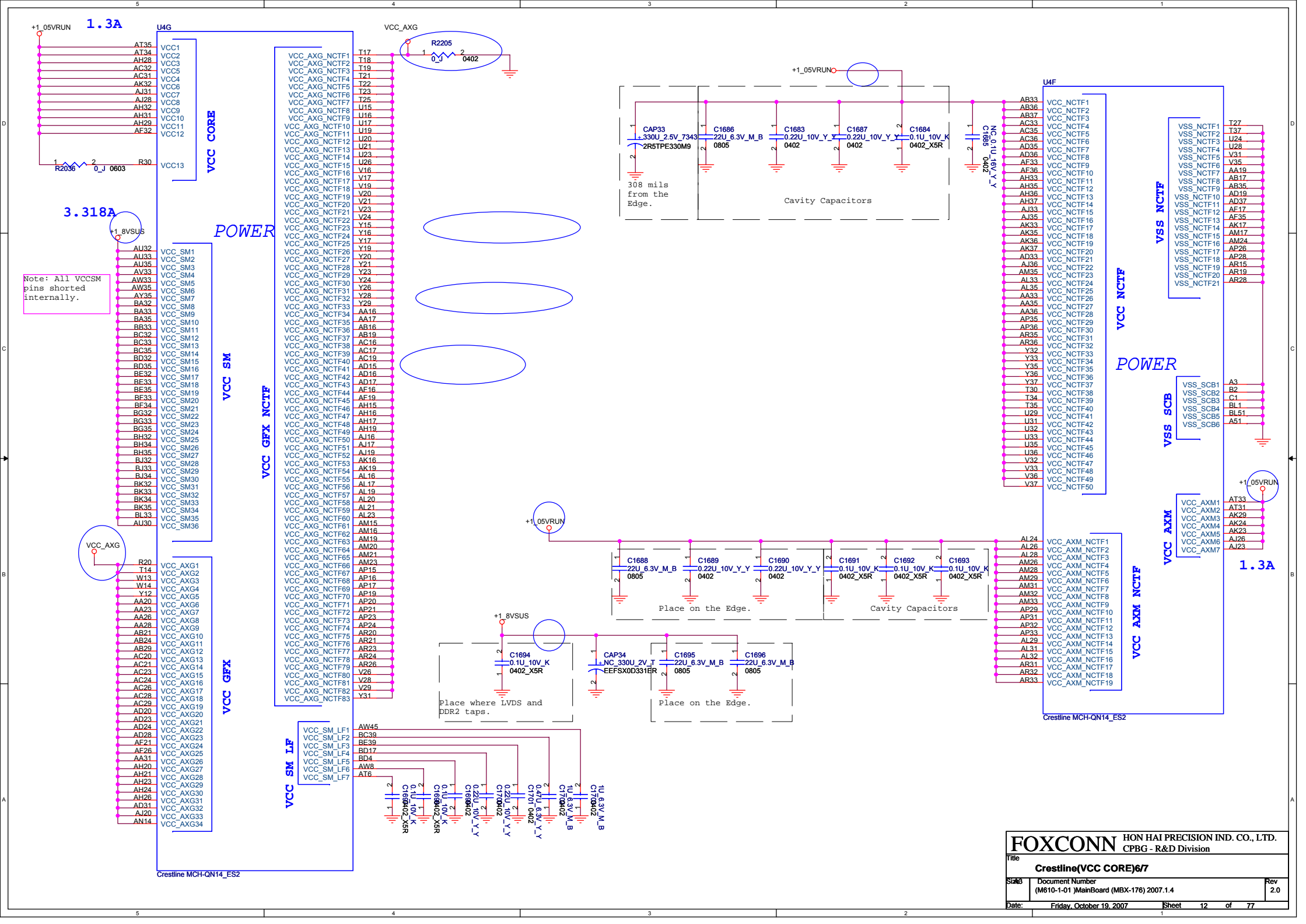
Size
A3 Document Number

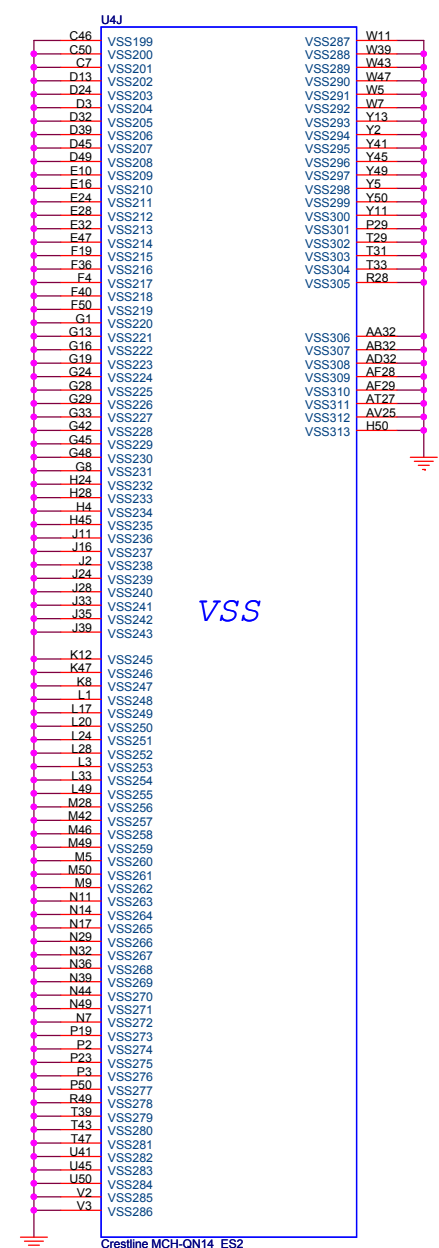
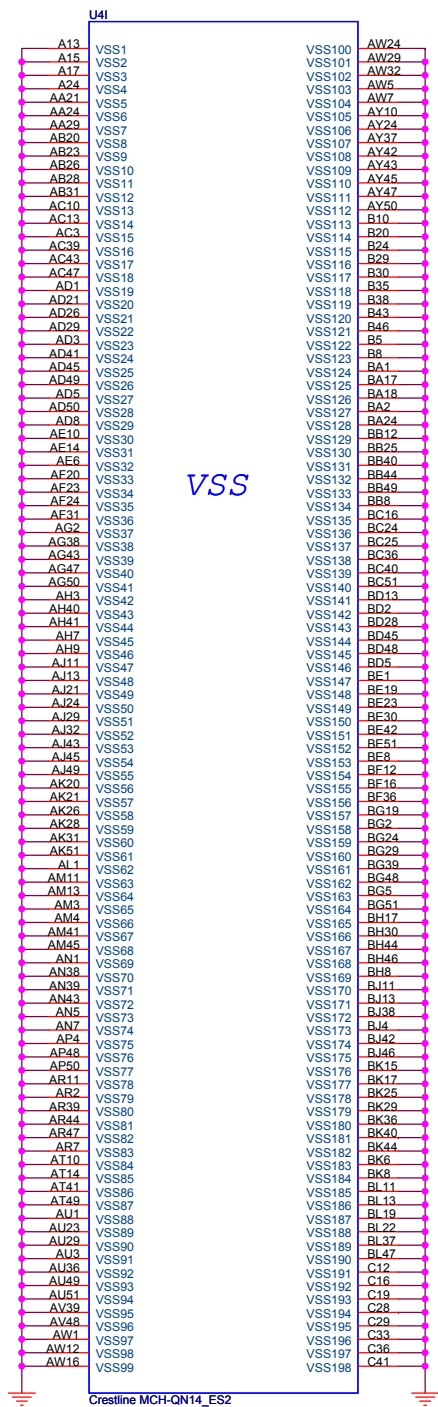
Date
FEBRUARY 19, 2007

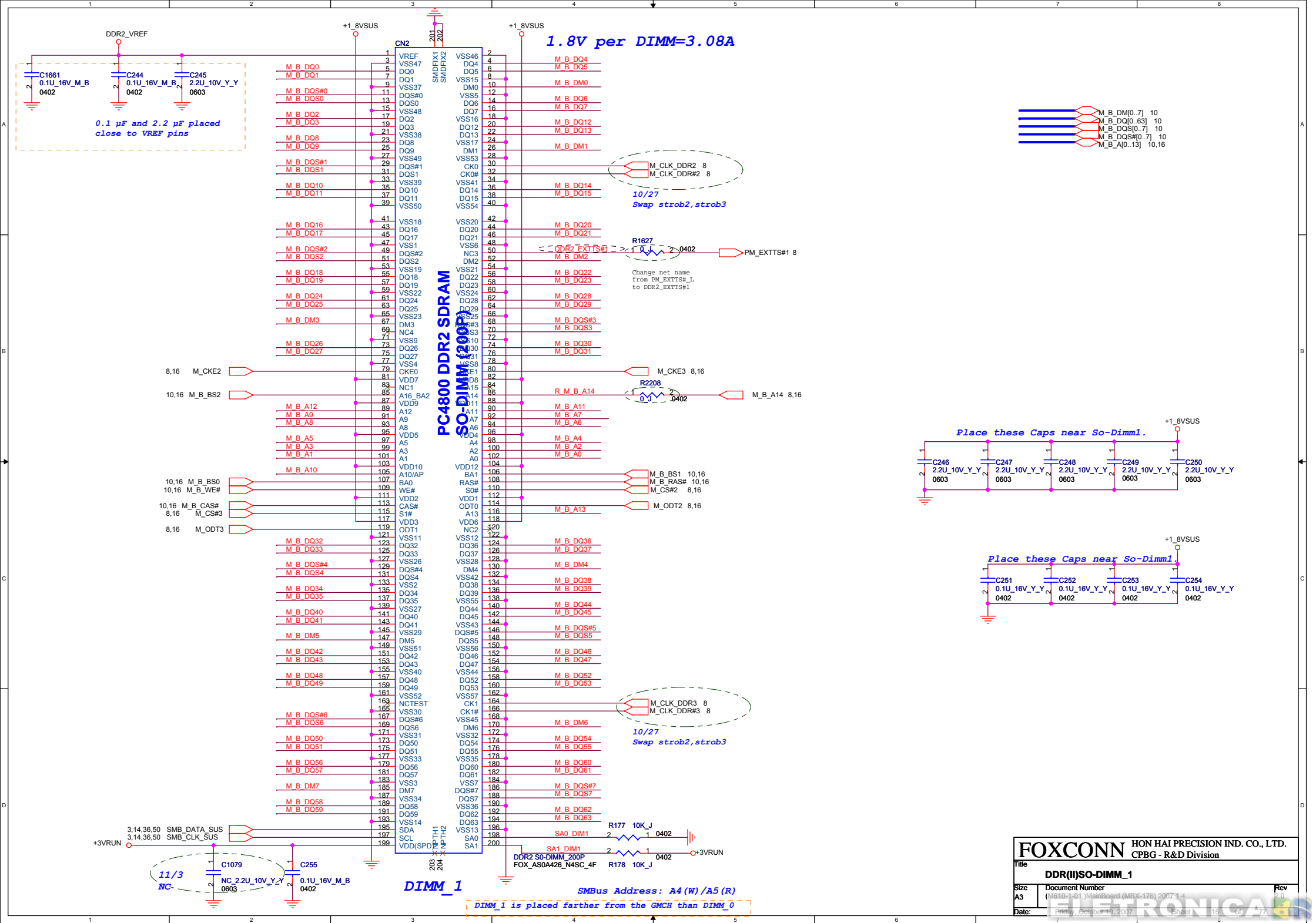
Rev
2.0

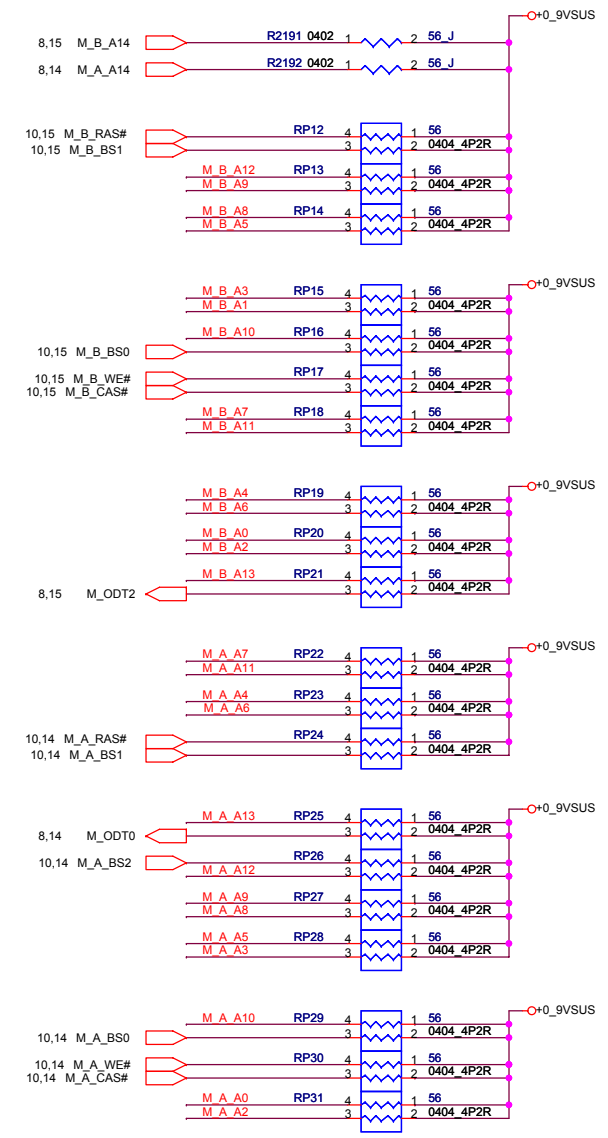
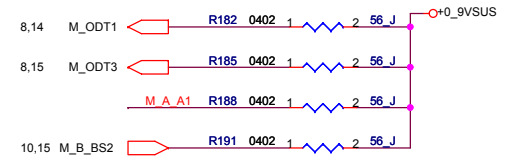
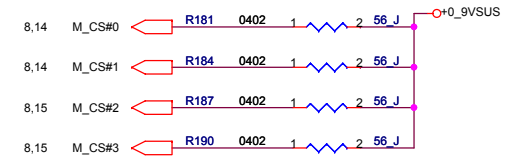
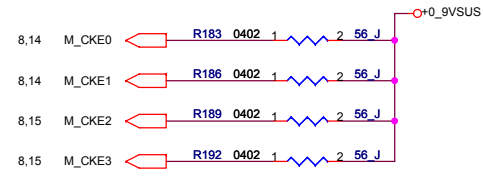
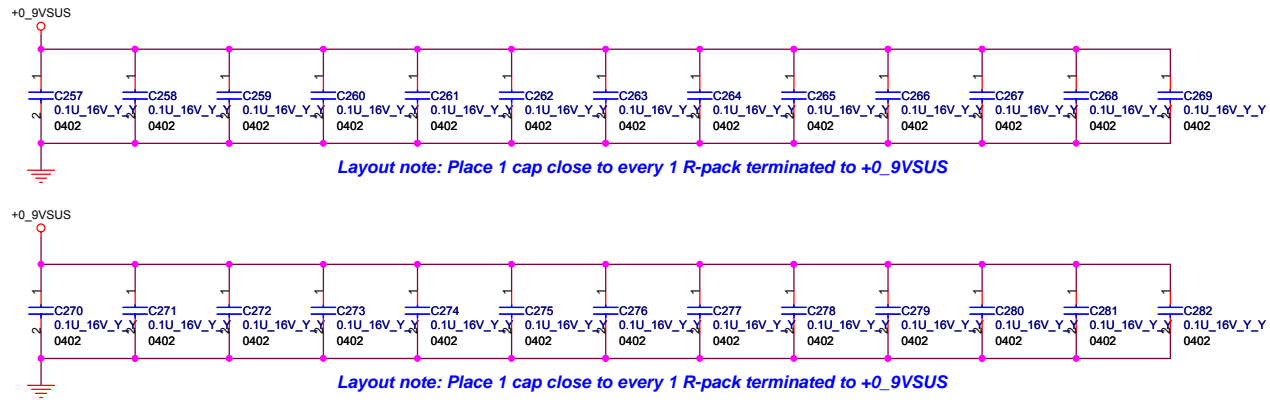


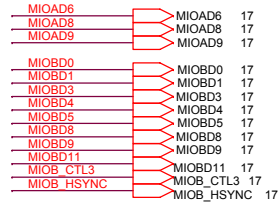
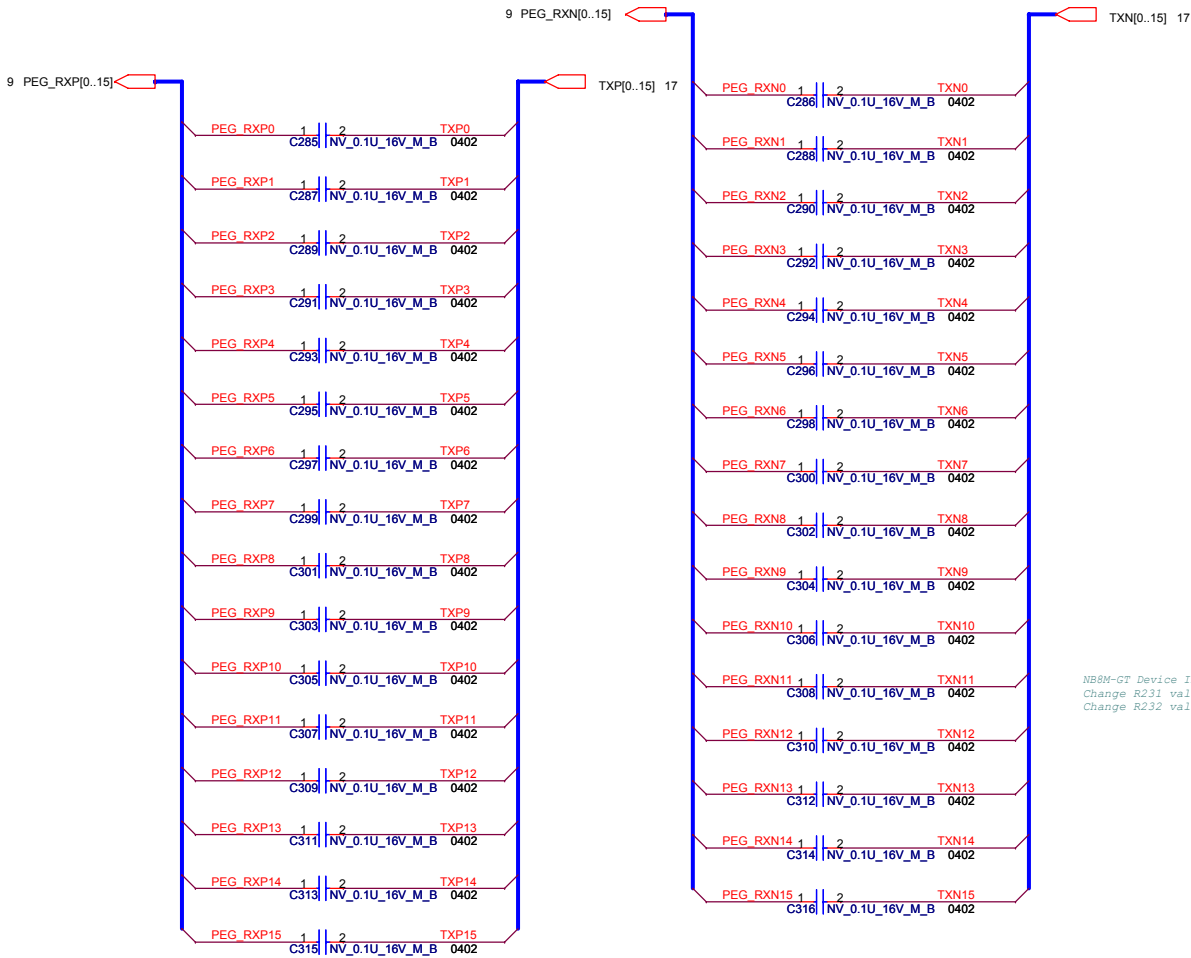












NB8X Strap for GDDR3-136ball

0001 16Mx32Infineon
0010 16Mx32Hynix
0011 16Mx32Samsung
0101 8Mx32Infineon
0110 8Mx32Hynix
0111 8Mx32Samsung

SUB_VENDOR

0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

MIOAD0 is used to set the PCI Express PLL termination enable.

DEFAULT "0"

NB8X 3GIO_PADCFG[3:0]

0001

NB8M-GT Device ID setting mismatch between VBIOS and H/W Straps
Change R231 value from NC_ to NV8M_
Change R232 value from NV_ to NV8P_

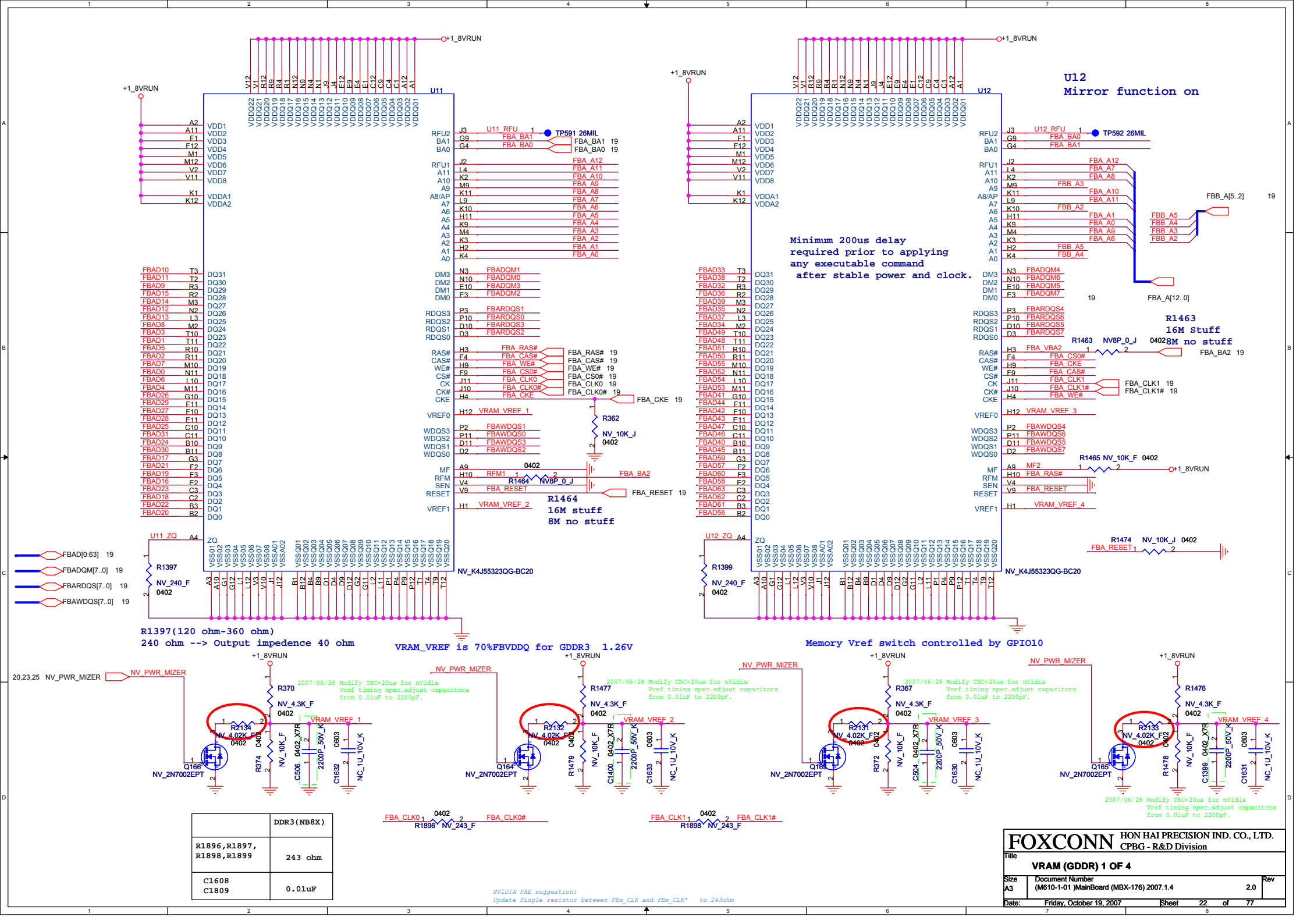
NB8X PCI_DEVID[4:0]

NB8P-GS X0111 "X7"
NB8M-GT X0110 "X6"

CRYSTAL (NB8X)

0 (27M Hz)
1 (Reserved)





U12
Mirror function on

Minimum 200us delay
required prior to applying
any executable command
after stable power and clock.

R1463
16M Stuff
no stuff

R1464
16M stuff
8M no stuff

Memory Vref switch controlled by GPIO10

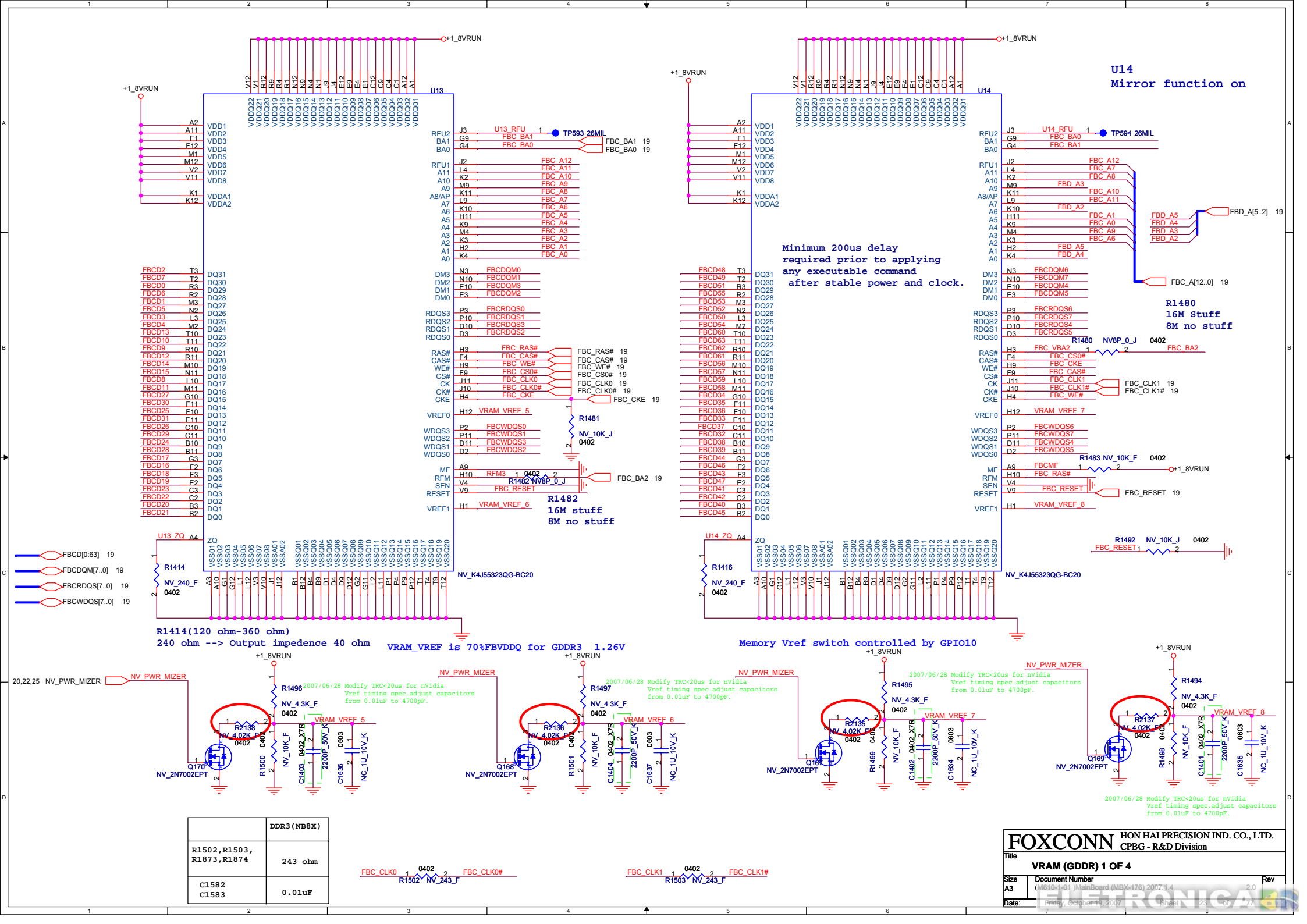
R1397(120 ohm-360 ohm)
240 ohm --> Output impedance 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

	DDR3 (NB8X)
R1896,R1897, R1898,R1899	243 ohm
C1608 C1809	0.01uF

NVIDIA FAE suggestion:
Update Single resistor between FBX_CLK and FBX_CLK# to 243ohm

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	DDR3 (NB8X)
R1502, R1503, R1873, R1874	243 ohm
C1582 C1583	0.01uF

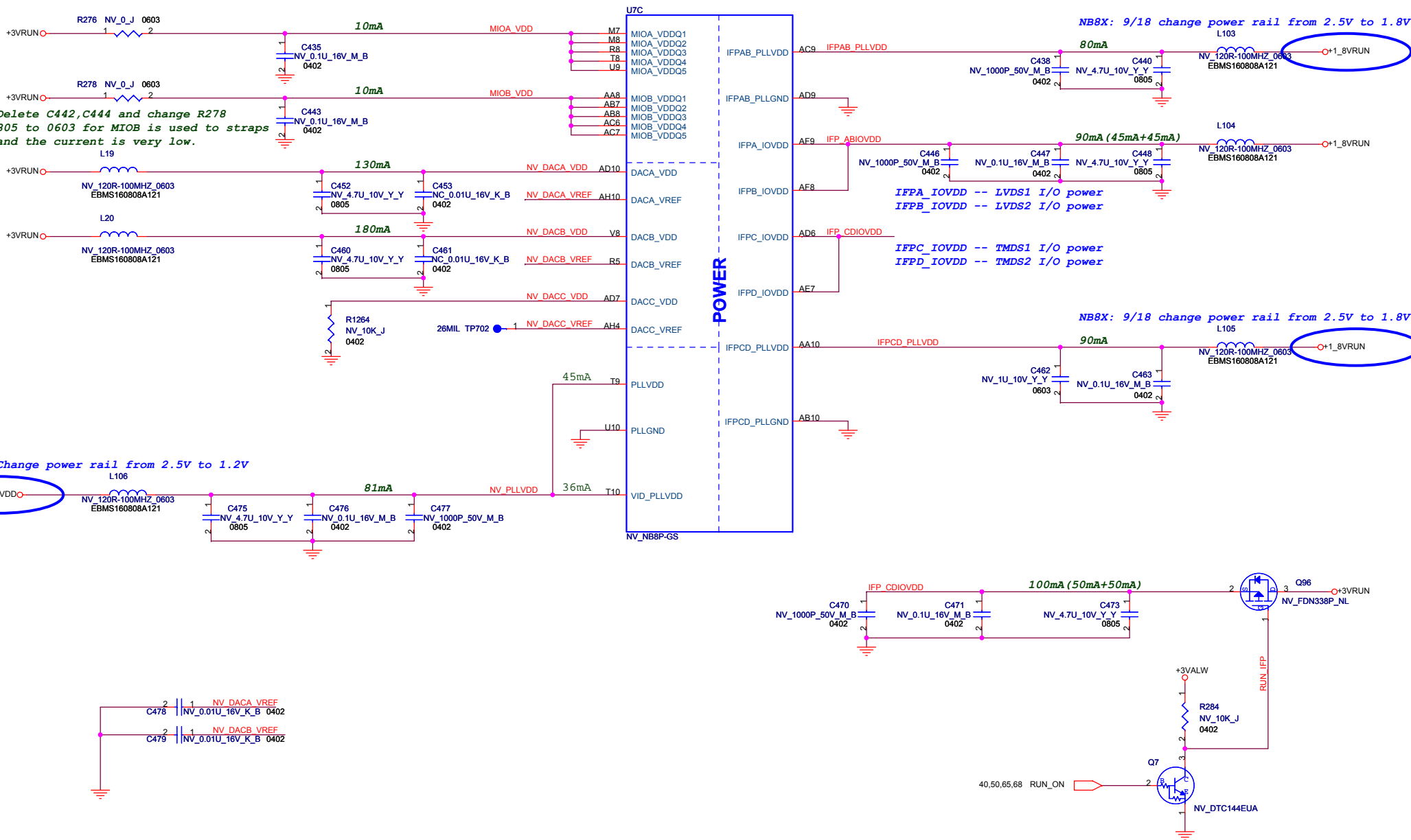
10/17 Delete C442, C444 and change R278 from 0805 to 0603 for MIOB is used to straps input and the current is very low.

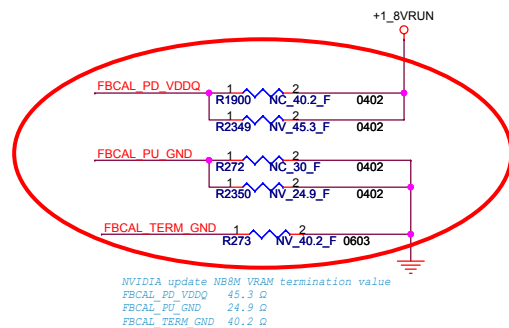
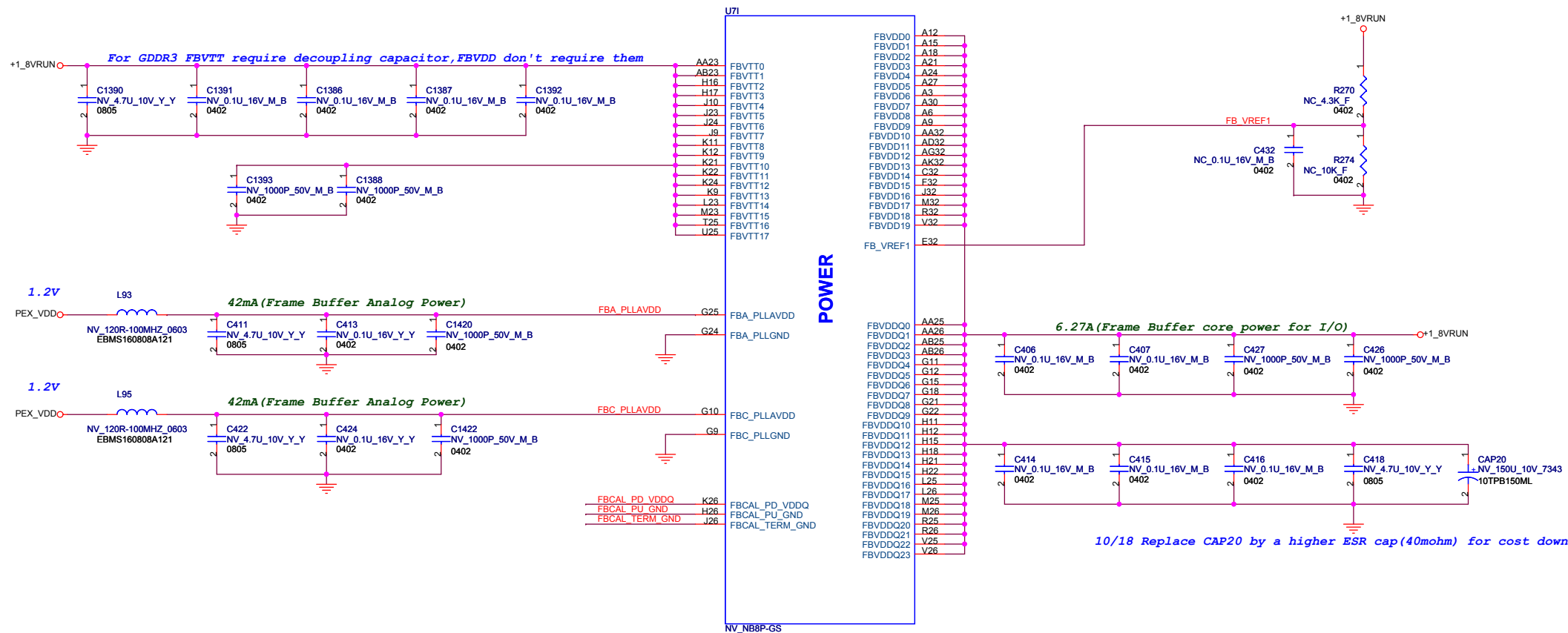
NB8X: Change power rail from 2.5V to 1.2V

NB8X: 9/18 change power rail from 2.5V to 1.8V

NB8X: 9/18 change power rail from 2.5V to 1.8V

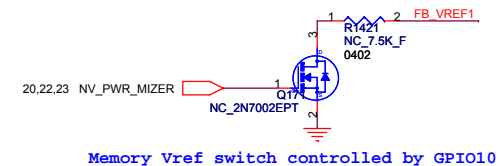
POWER

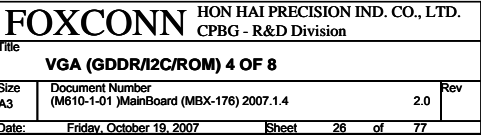




NVIDIA 07/1/5 update

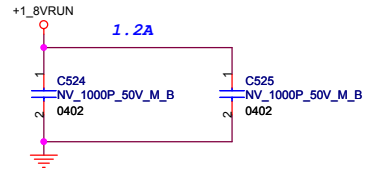
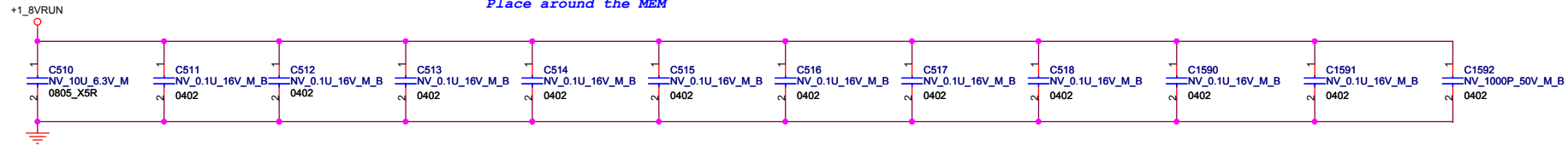
	DDR3 (NB8M-GT)	DDR3 (NB8P-GS)
FBCAL_PD_VDDQ	45.3 ohm	45.3 ohm
FBCAL_PU_GND	24.9 ohm	24.9 ohm
FBCAL_TERM_GND	40.2 ohm	40.2 ohm





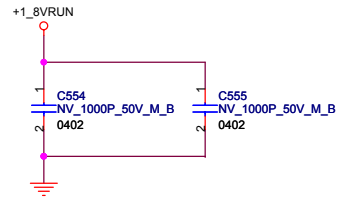
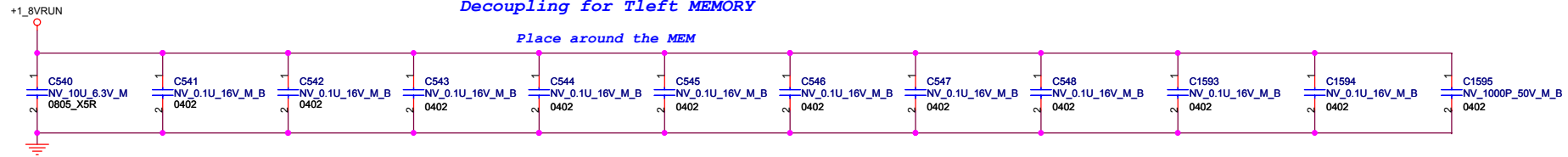
Decoupling for Tright MEMORY

Place around the MEM



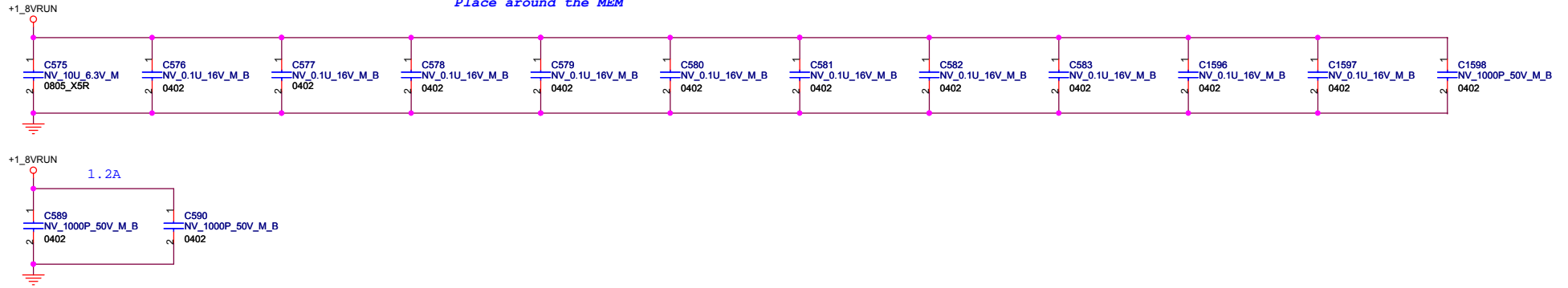
Decoupling for Tleft MEMORY

Place around the MEM



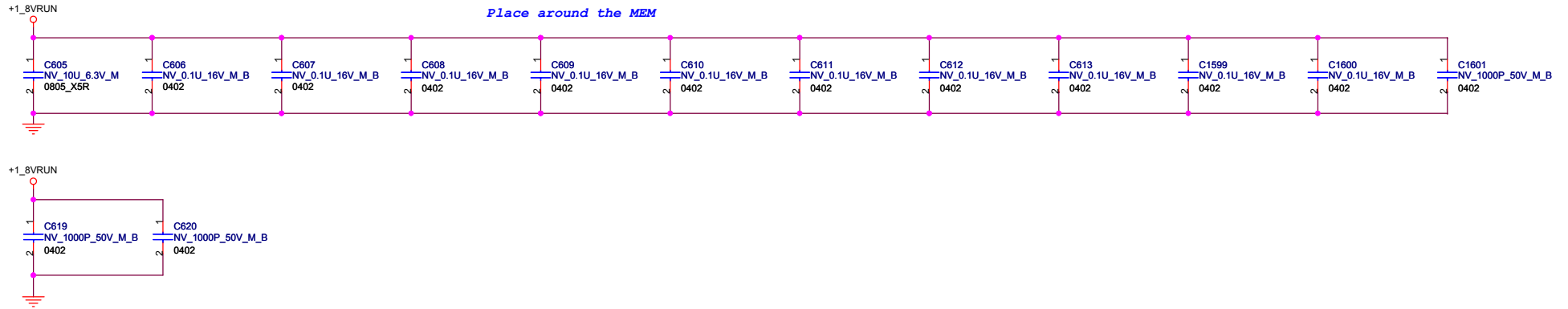
Decoupling for Bright MEMORY

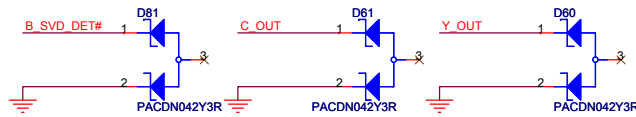
Place around the MEM



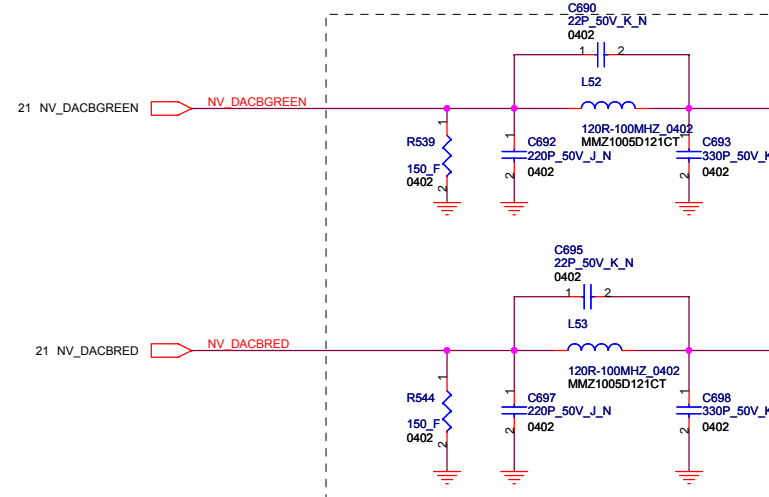
Decoupling for Bleft MEMORY

Place around the MEM

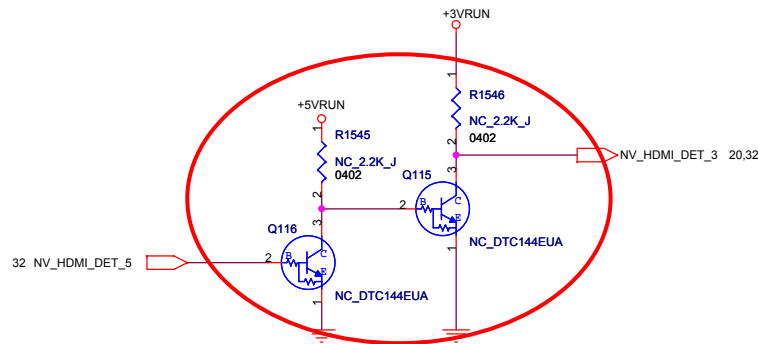
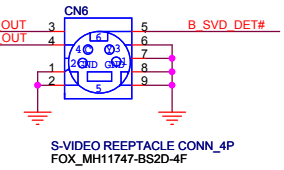




These component close to S-Video connector within 700 mil

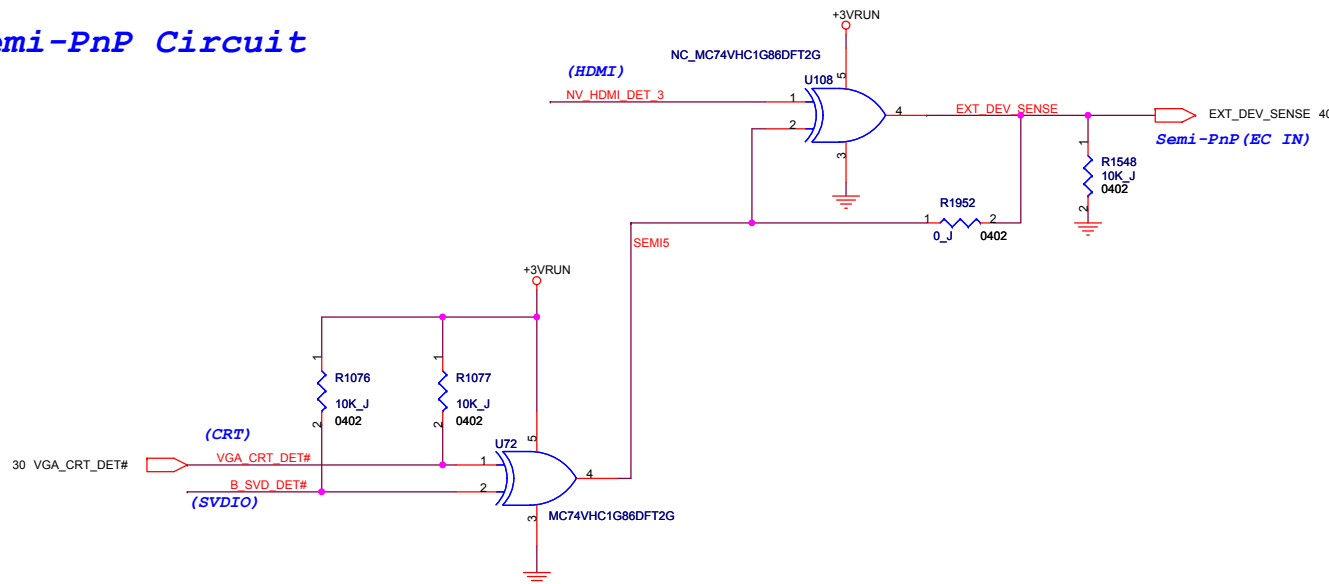


S-VIDEO CONNECTOR

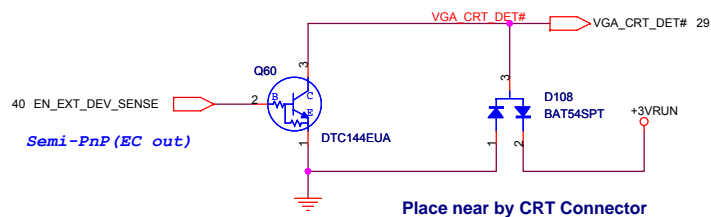


PS101 HPD has level shift function, so backup this circuit
Change Q115, Q116, R1545, R1546 to NC

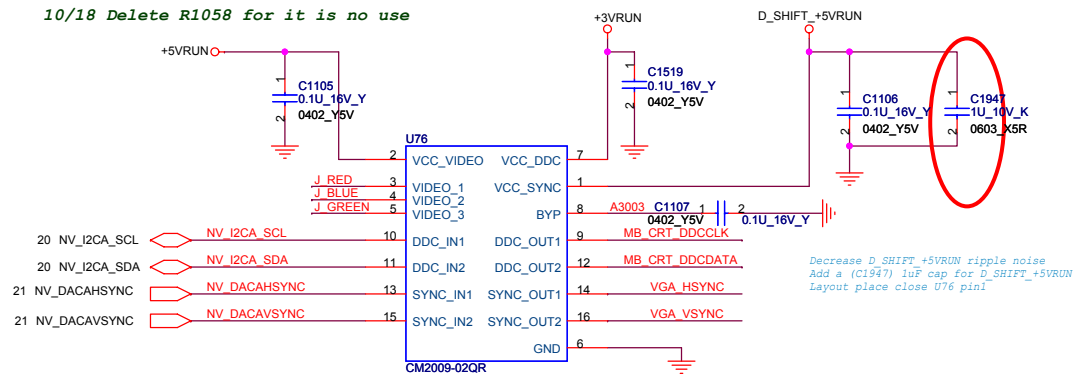
Semi-PnP Circuit



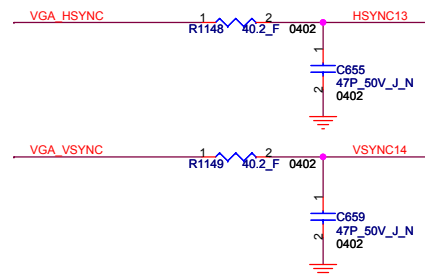
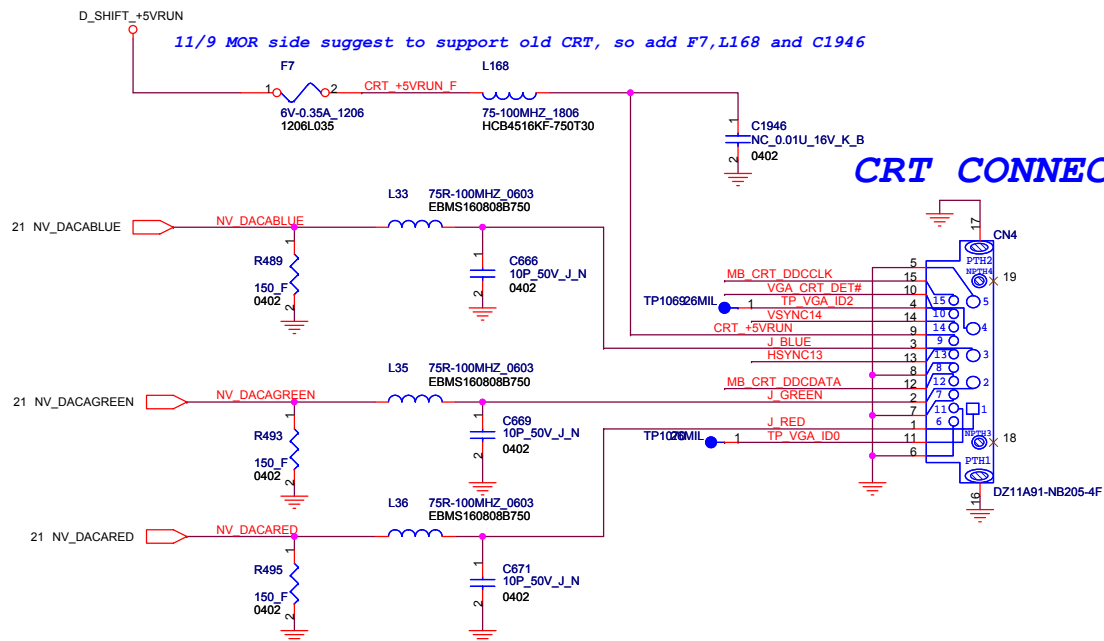
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CPBG - R&D Division		
Title		
S-VIDEO/Semi-PnP		
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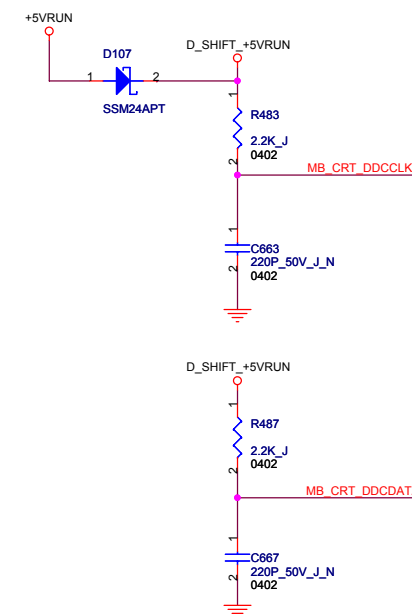
10/18 Delete R1058 for it is no use



11/9 MOR side suggest to support old CRT, so add F7, L168 and C1946

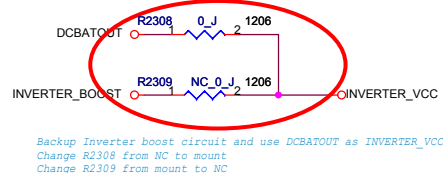
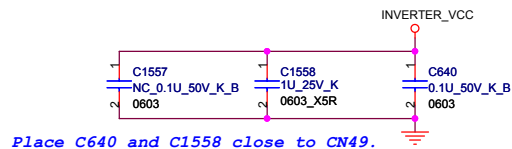


11/8 Change R1148, R1149 from 0ohm to 40ohm for meet CM2009-02 termination Spec

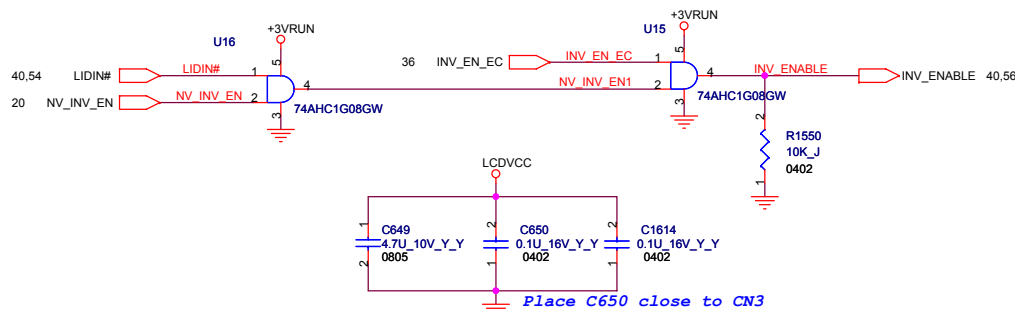
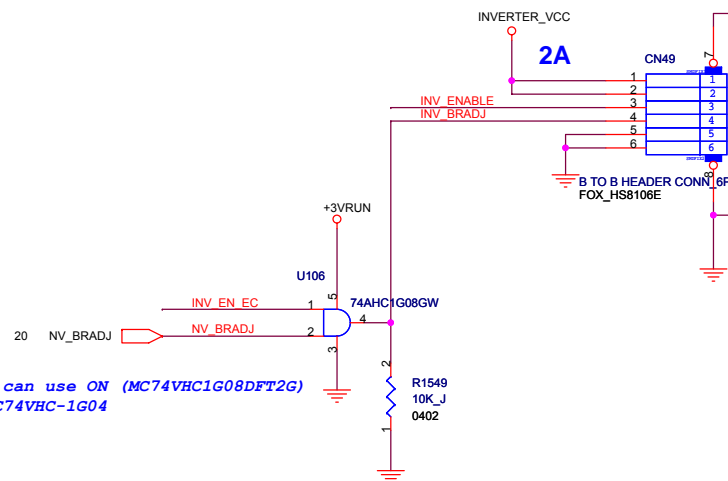


LVDS CONNECTOR

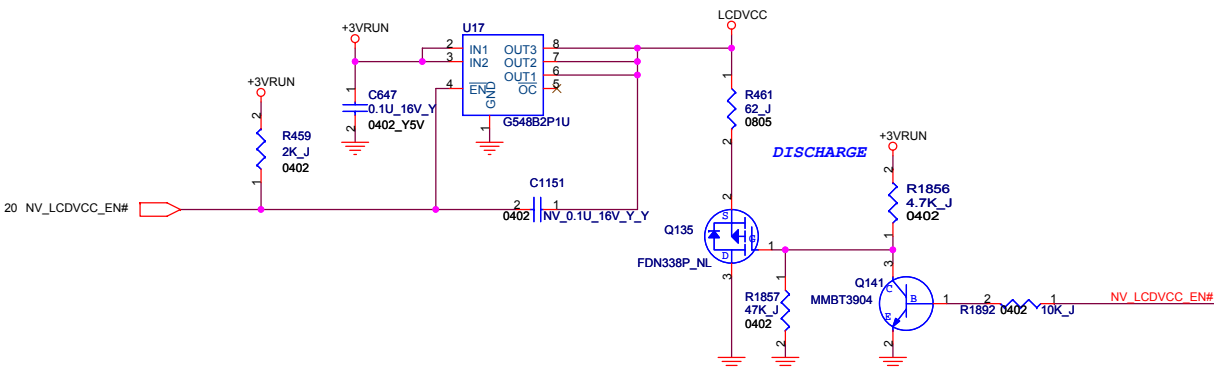
INVERTER CONNECTOR



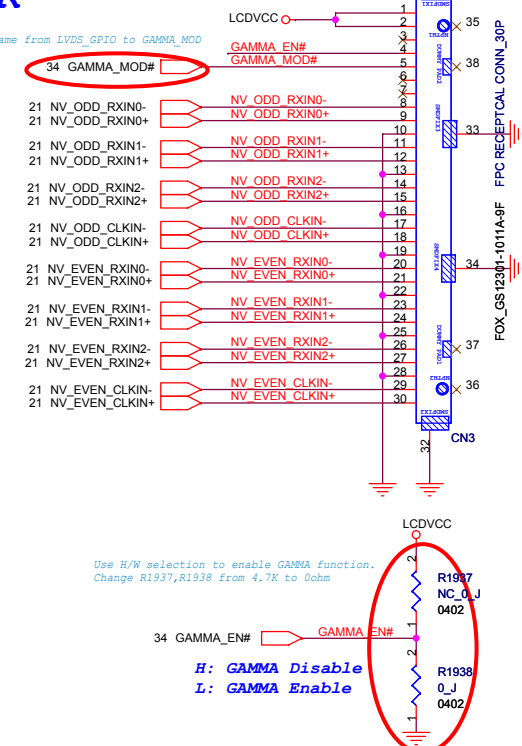
U106, U15, U16 can use ON (MC74VHC1G08DFT2G)
H.H. PN:14-MC74VHC-1G04



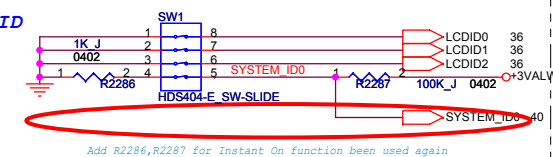
Current limit is from 1.1A to 2.1A.



Change net name from LVDS_GPIO to GAMMA_MOD



PANEL ID



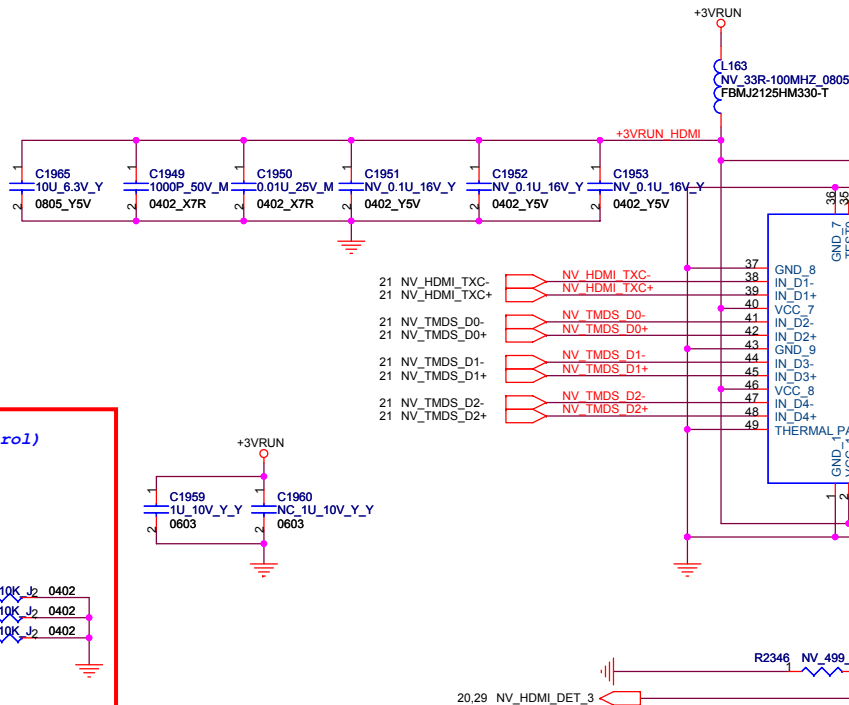
Type	WXGA+	WXGA+	WXGA	WXGA
Size	17" wide	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP	SHARP
Device Name	LPI171WP7-TLA	LPI171WP7-TLA	LQ170M1LA4G	LQ170M1LA4B
Panel ID Check[2..0]	010	001	100	101

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

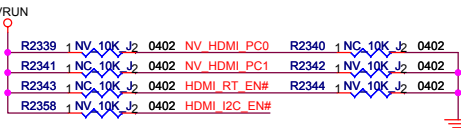
Title
LVDS

Size
A3

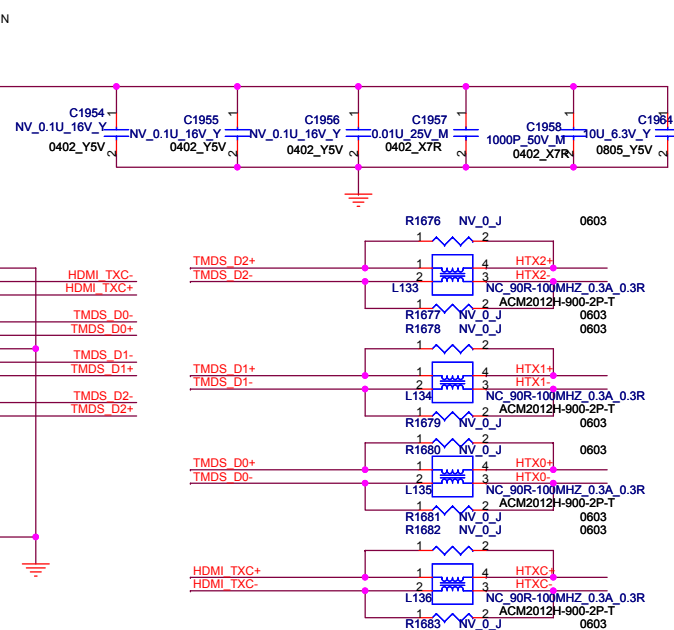
Date: Primary: October 19, 2007 Sheet: 31 of 77



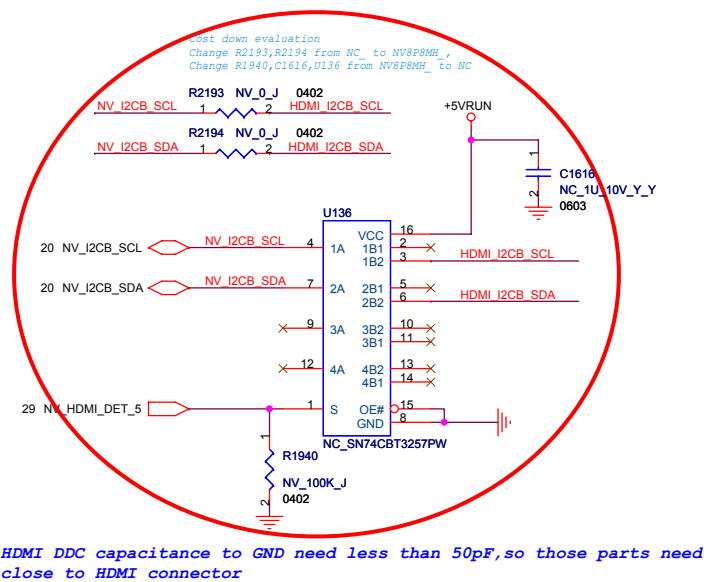
(TMDS inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB



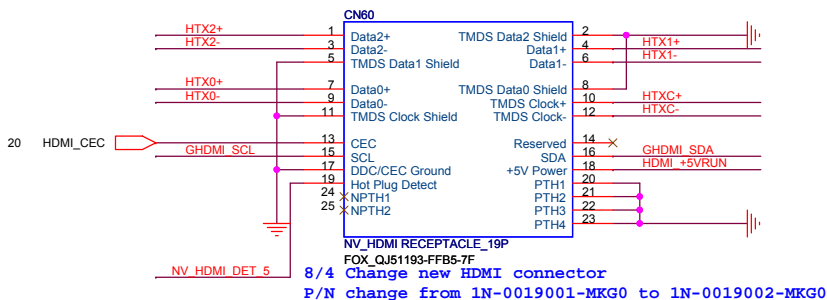
Add HDMI equalizer for M610 long trace issue



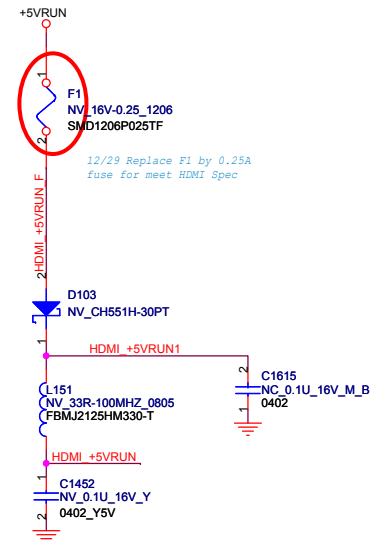
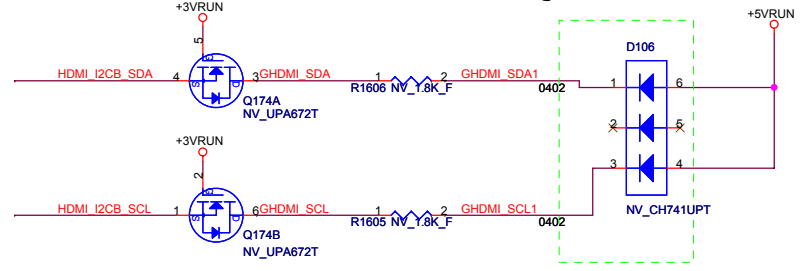
Data line capacitance to GND need less than 10pF,
so those parts need close to HDMI connector



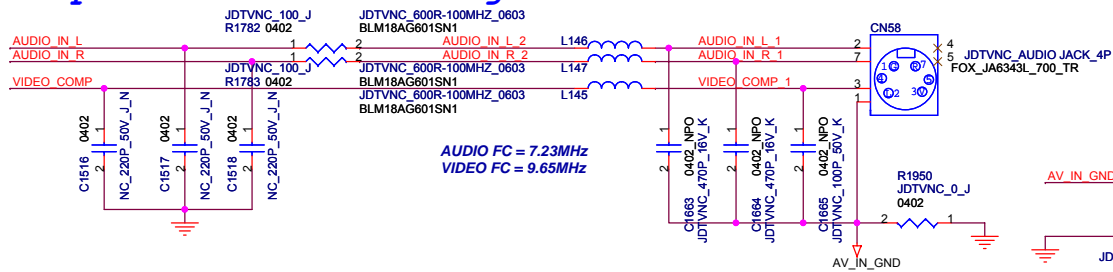
HDMI CONNECTOR



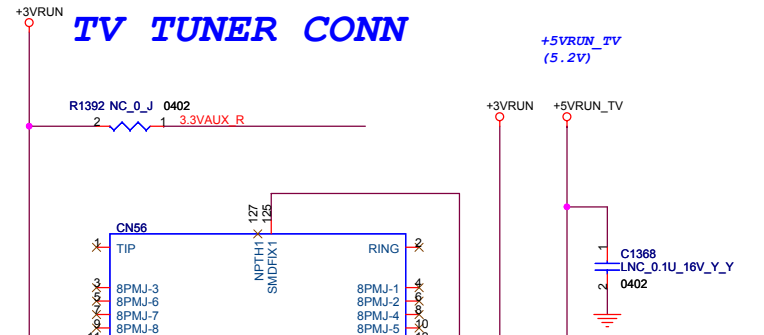
PVT Change to 16-CH741UP-T000



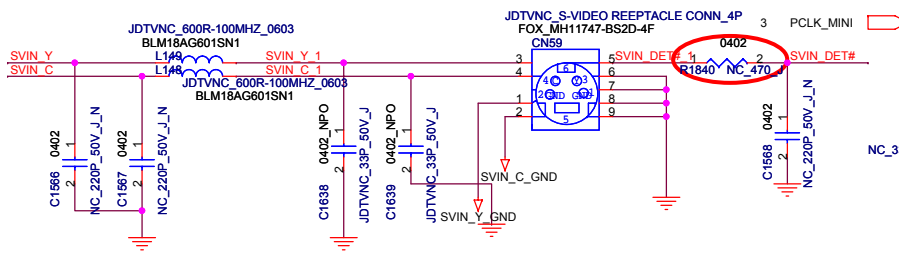
Special mini stereo jack



TV TUNER CONN

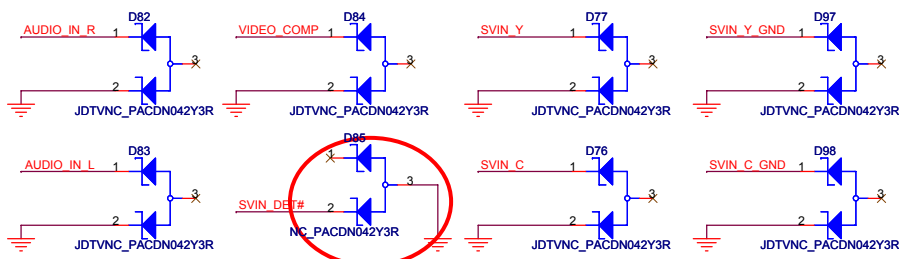


S-VIDEO IN



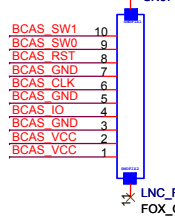
TV-TUNER not support CLKRUN

TV tuner "SVIN_DET#" signal no use.
Change R1840, D85 to NC



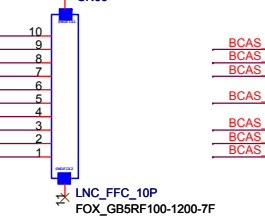
B-CAS connentor

(Close to TV Tuner)

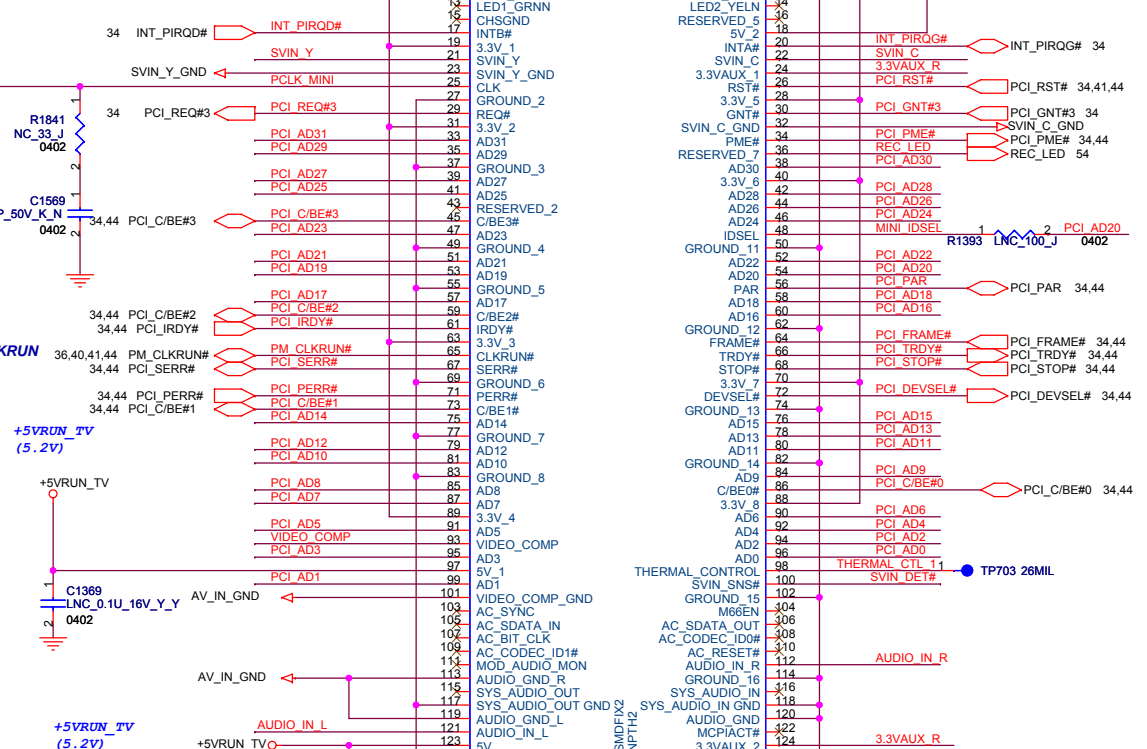
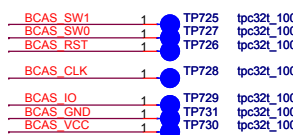


FFC CONNECT TO TV TUNER BOARD

(FOR JP DIAGITAL)

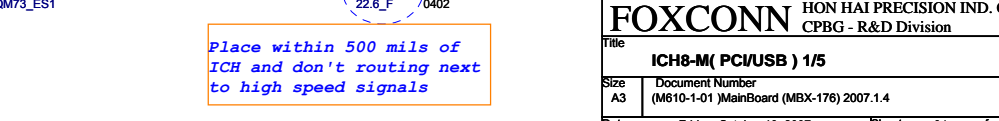
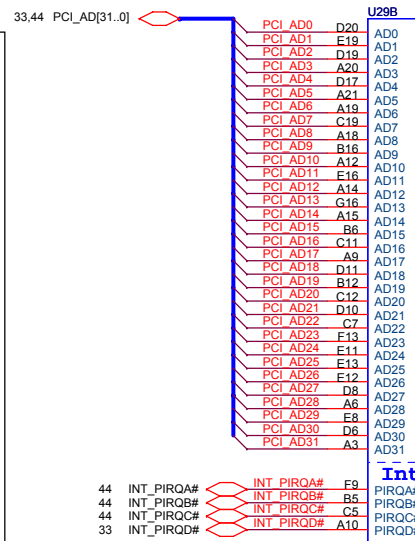


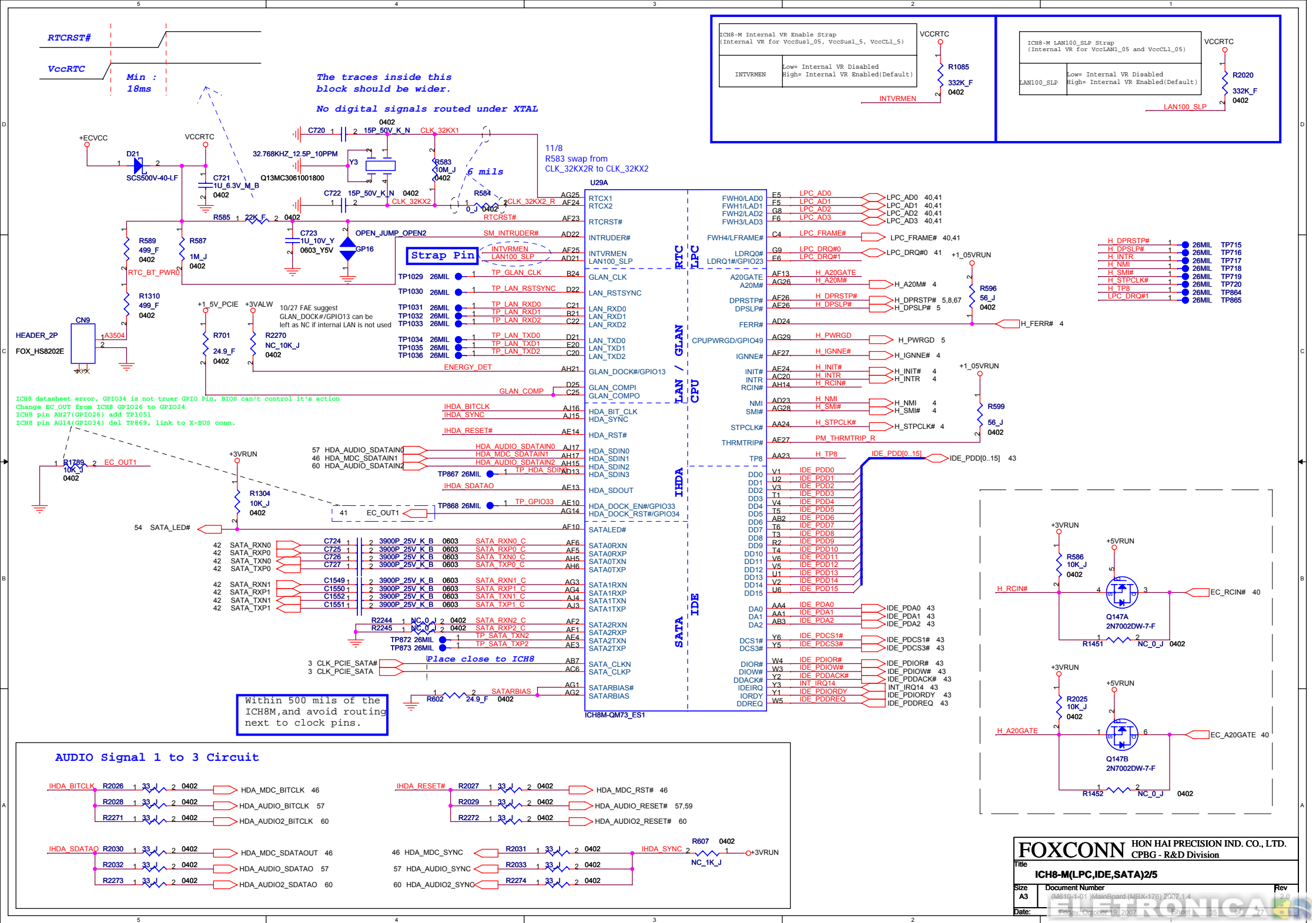
BFT Test Pad

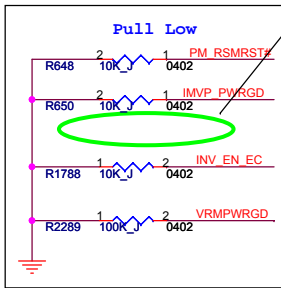
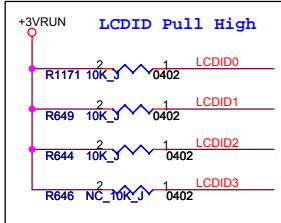
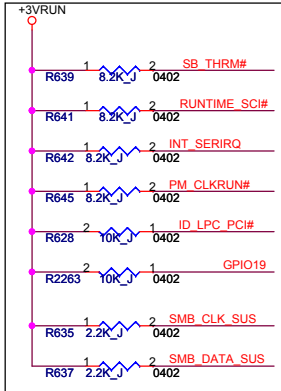
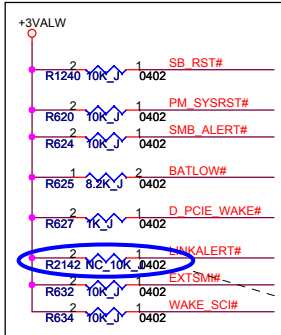
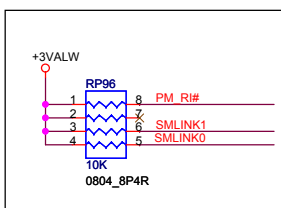


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title	MINI-PCI CONN.
Size	Document Number
Date	1/18/10-1/01 (MainBoard (MBX-176) 2007.1.4
	Primary October 19, 2007
	Sheet 33 of 77





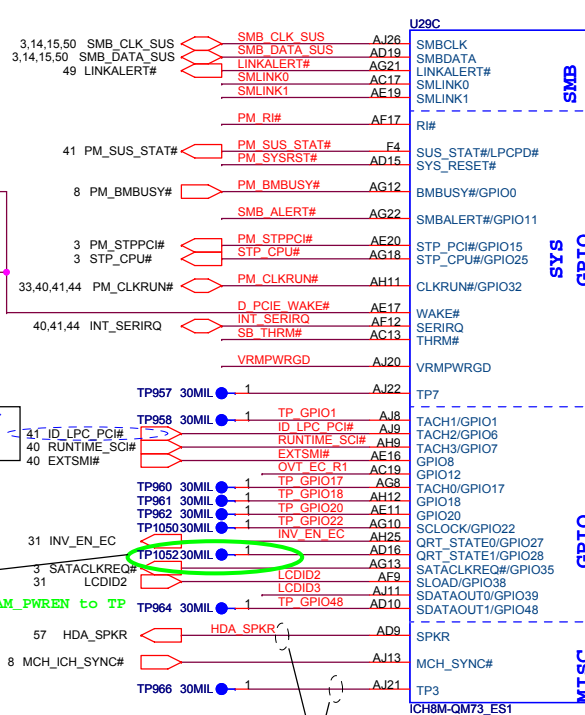


10/27 FAE suggest
No stuff R2142. LINKALERT# can
be left as NC if unused this function.
See Santa Rosa MOW WW33

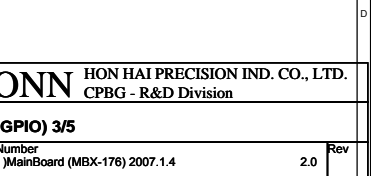
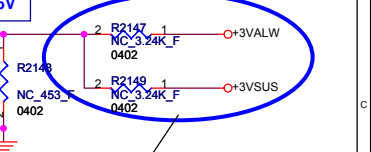
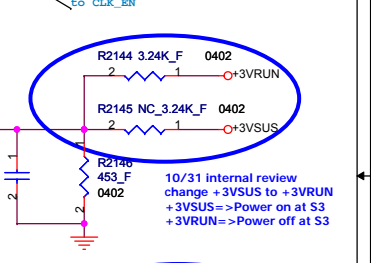
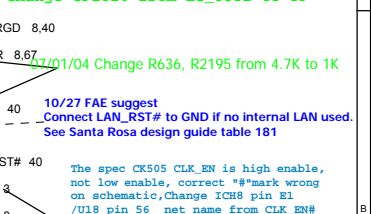
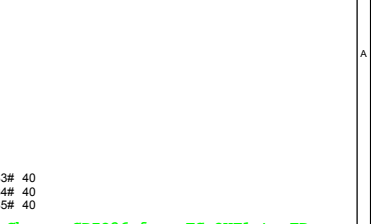
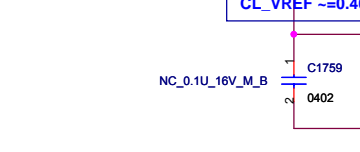
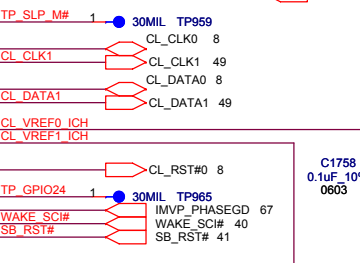
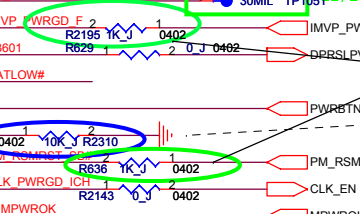
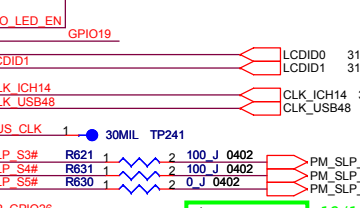
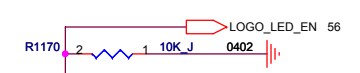
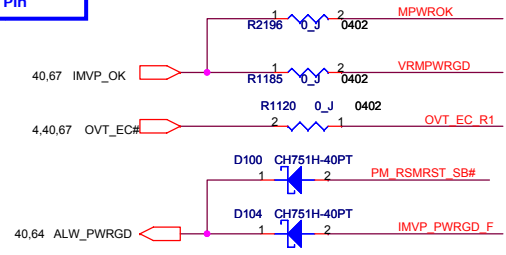
80 Port I/F:
H: LPC bus
L: PCI bus

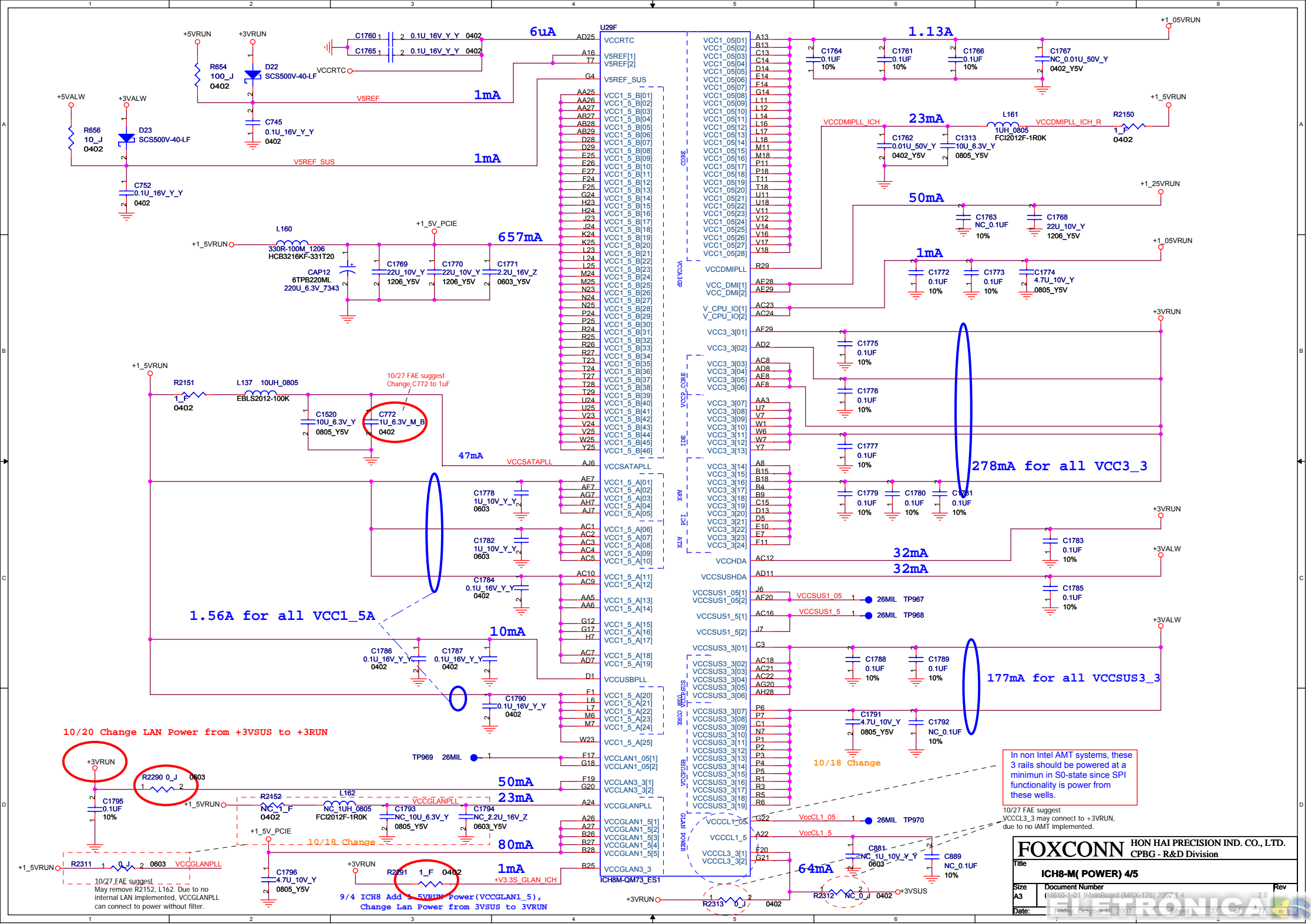
12/27 Change GPIO28 Net from CAM_PWREN to TP

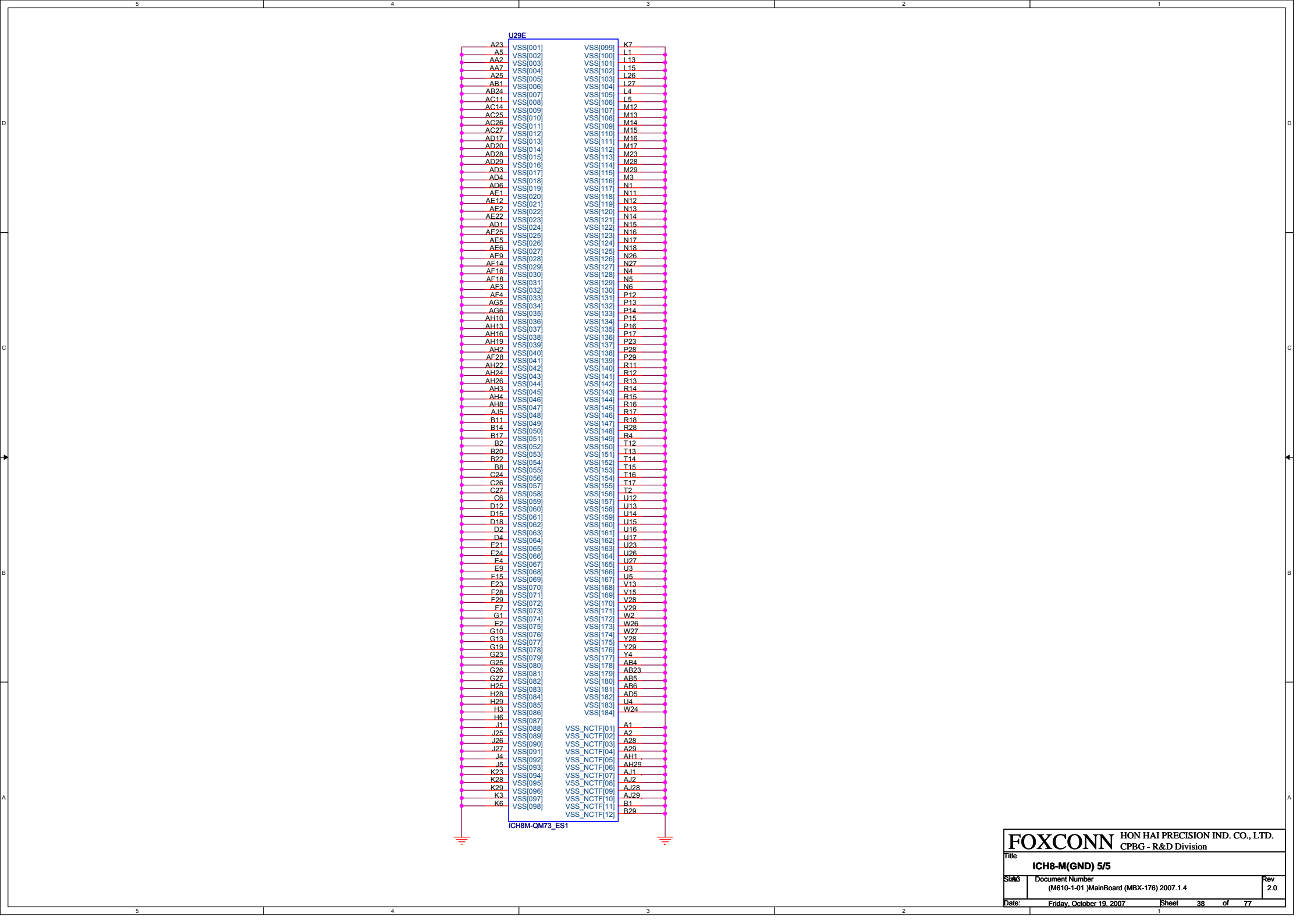
12/27 Delete R1787

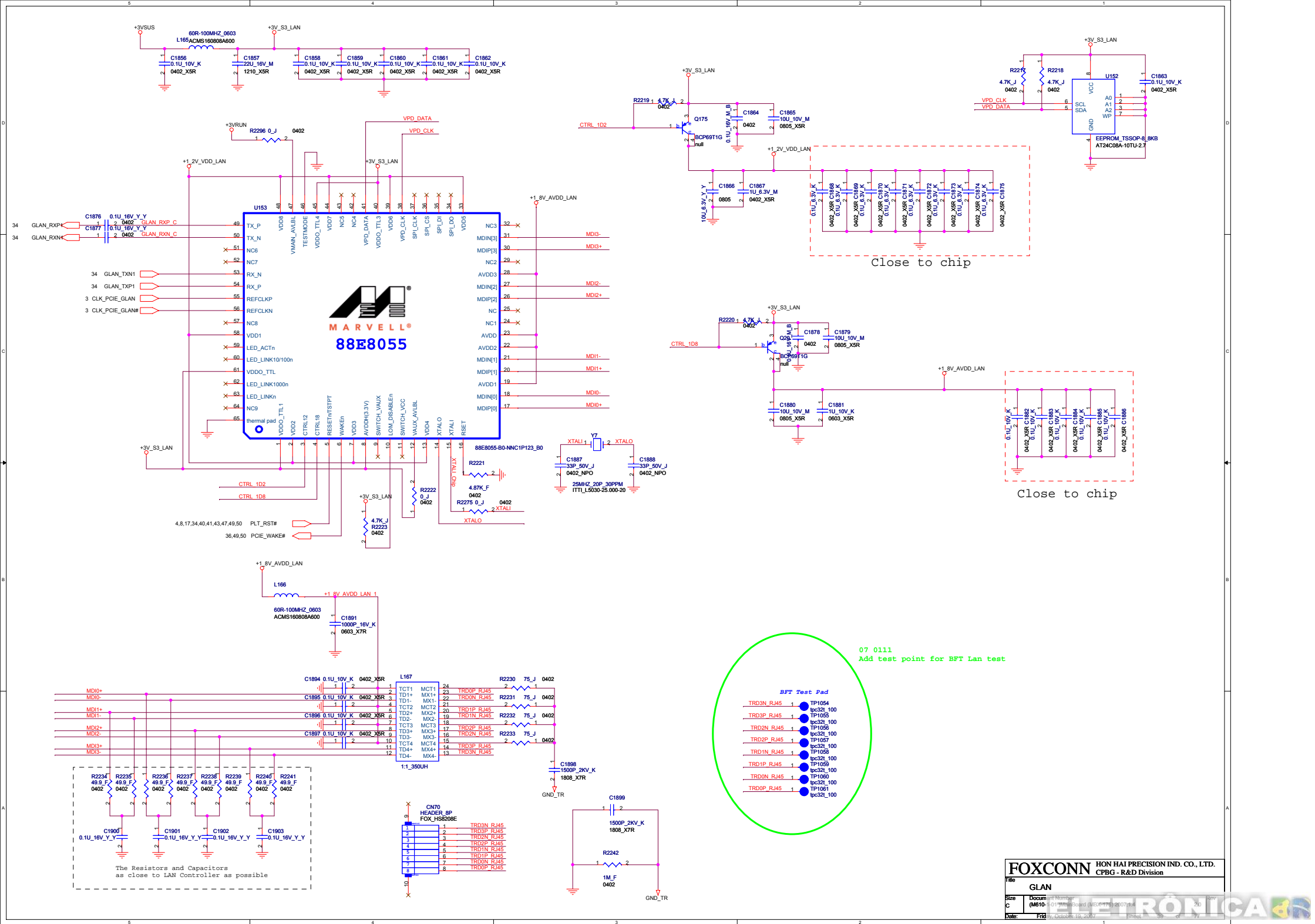


Straps Pin





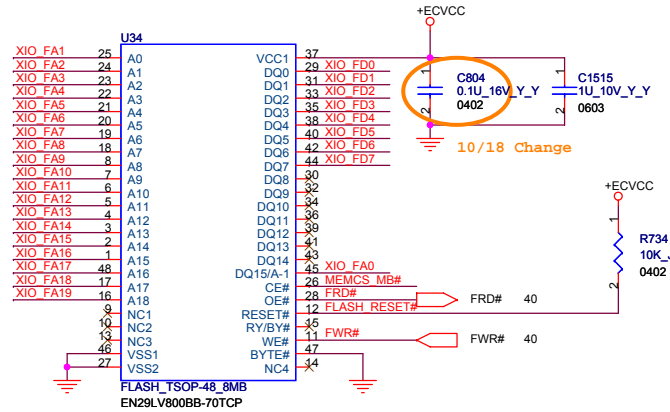




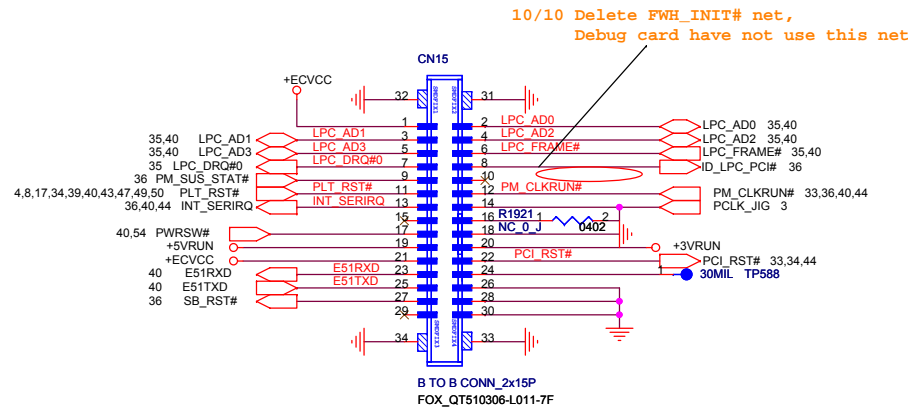
40 XIO_FA[19..0]

40 XIO_FD[7..0]

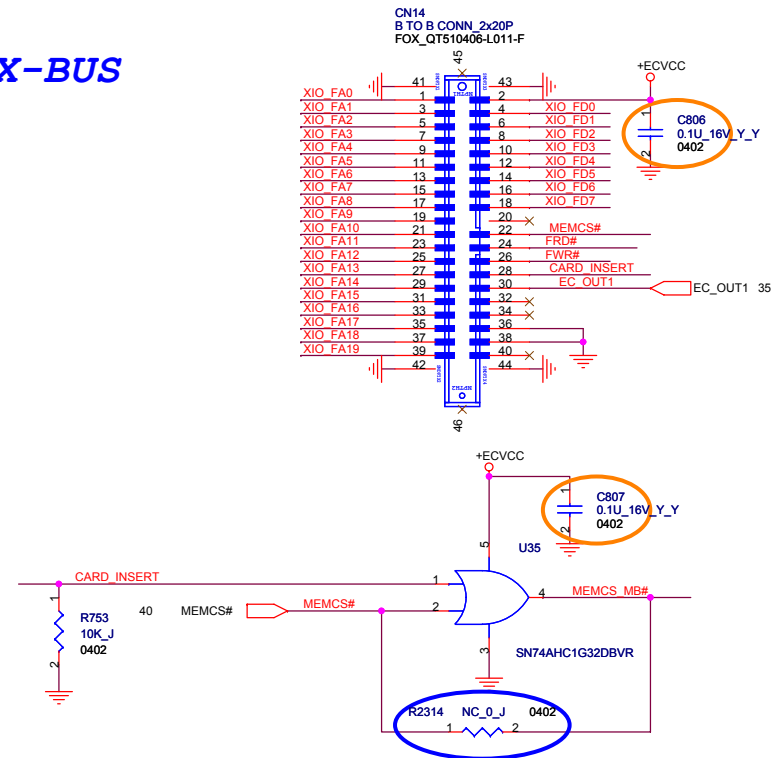
FLASH BIOS

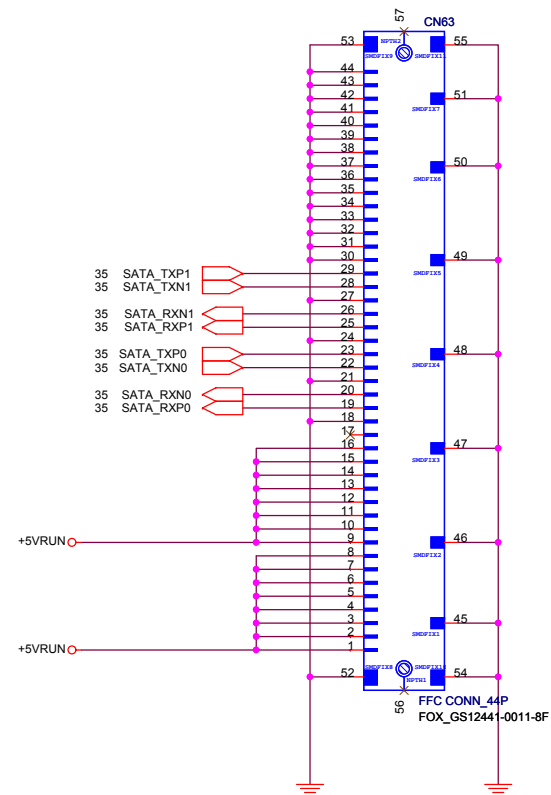
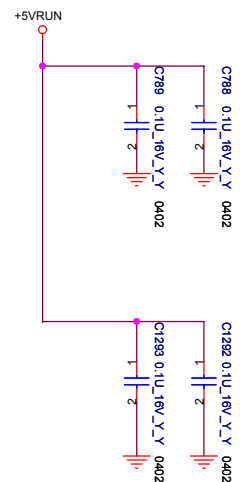


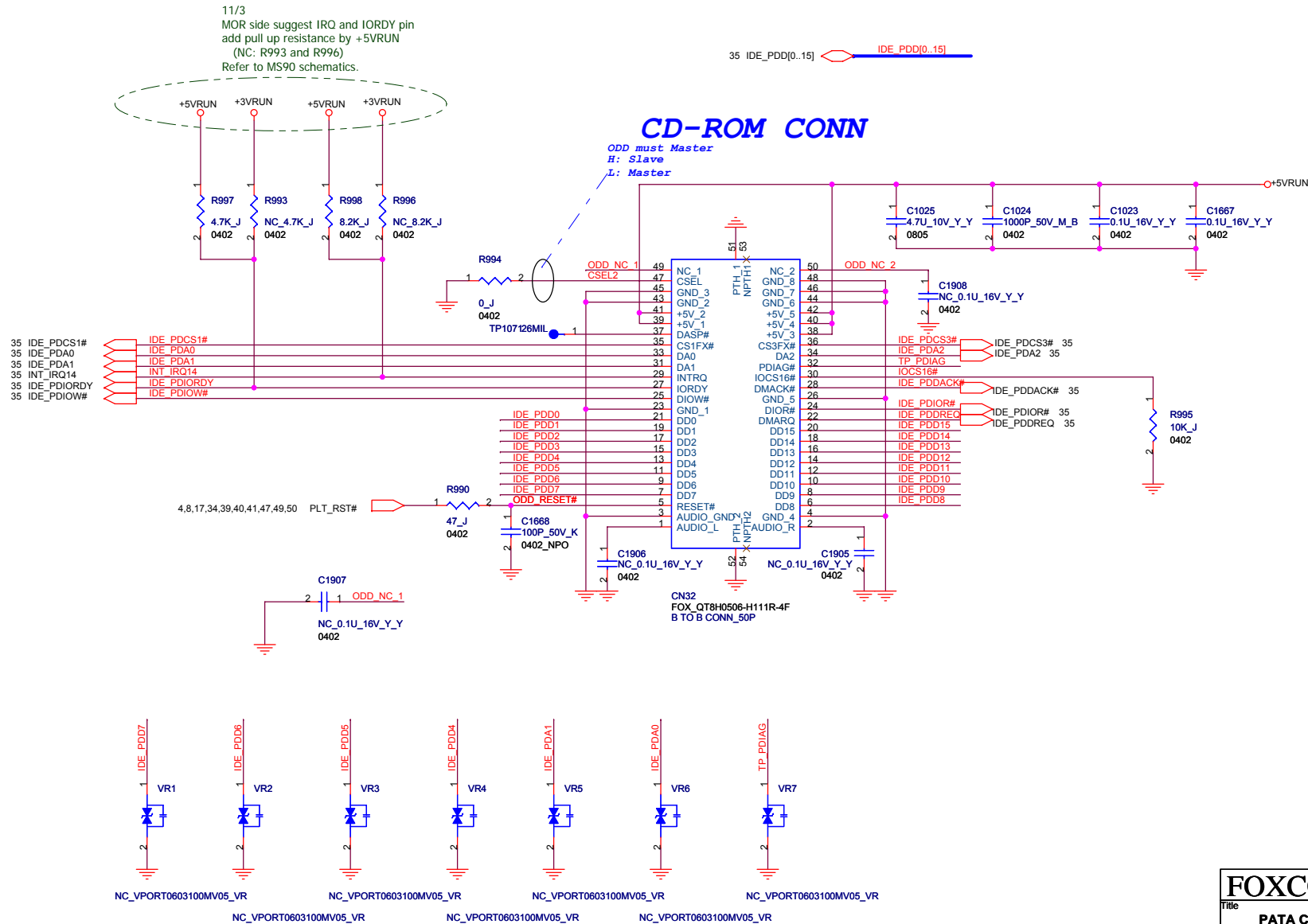
JIG-120

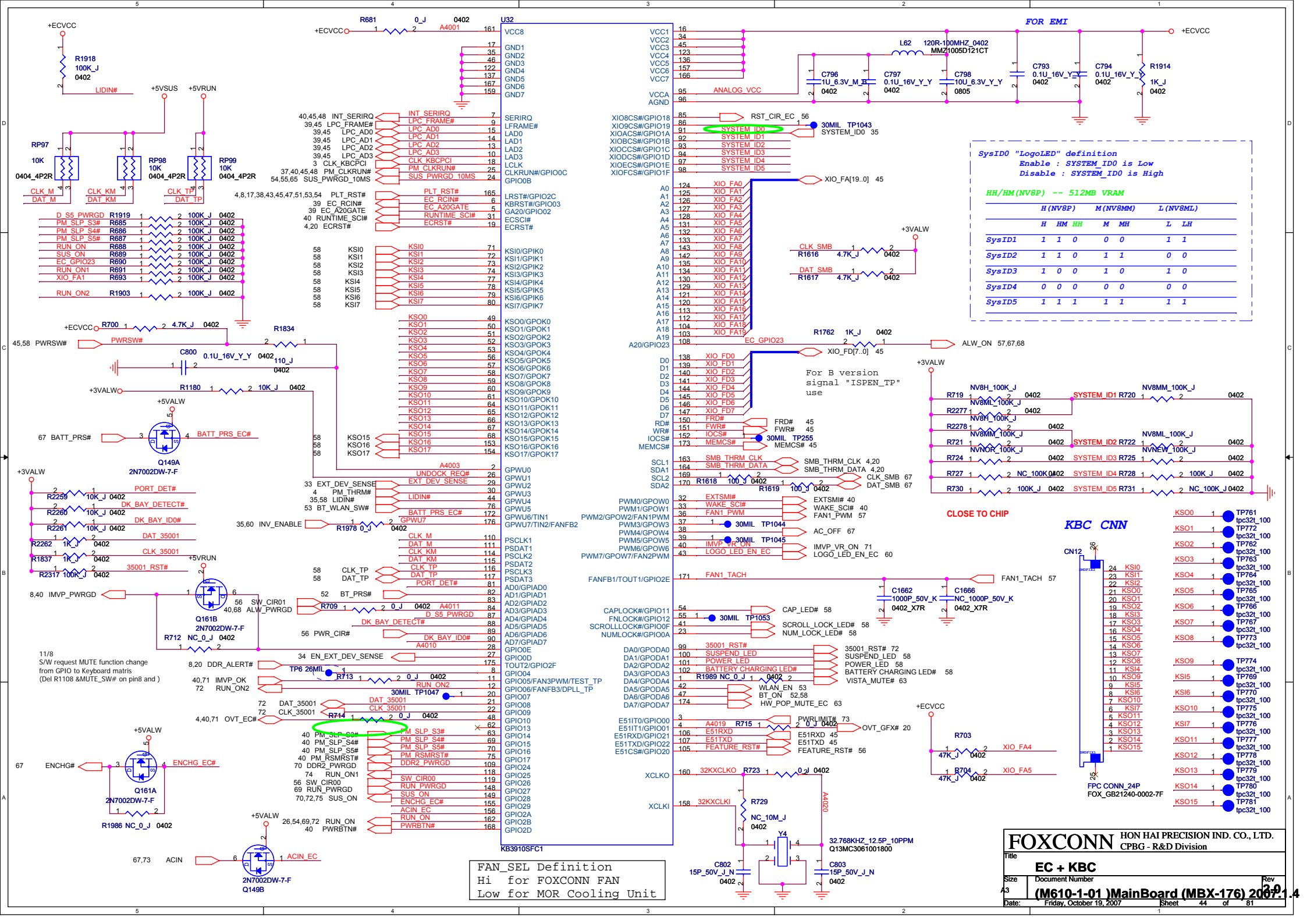


X-BUS

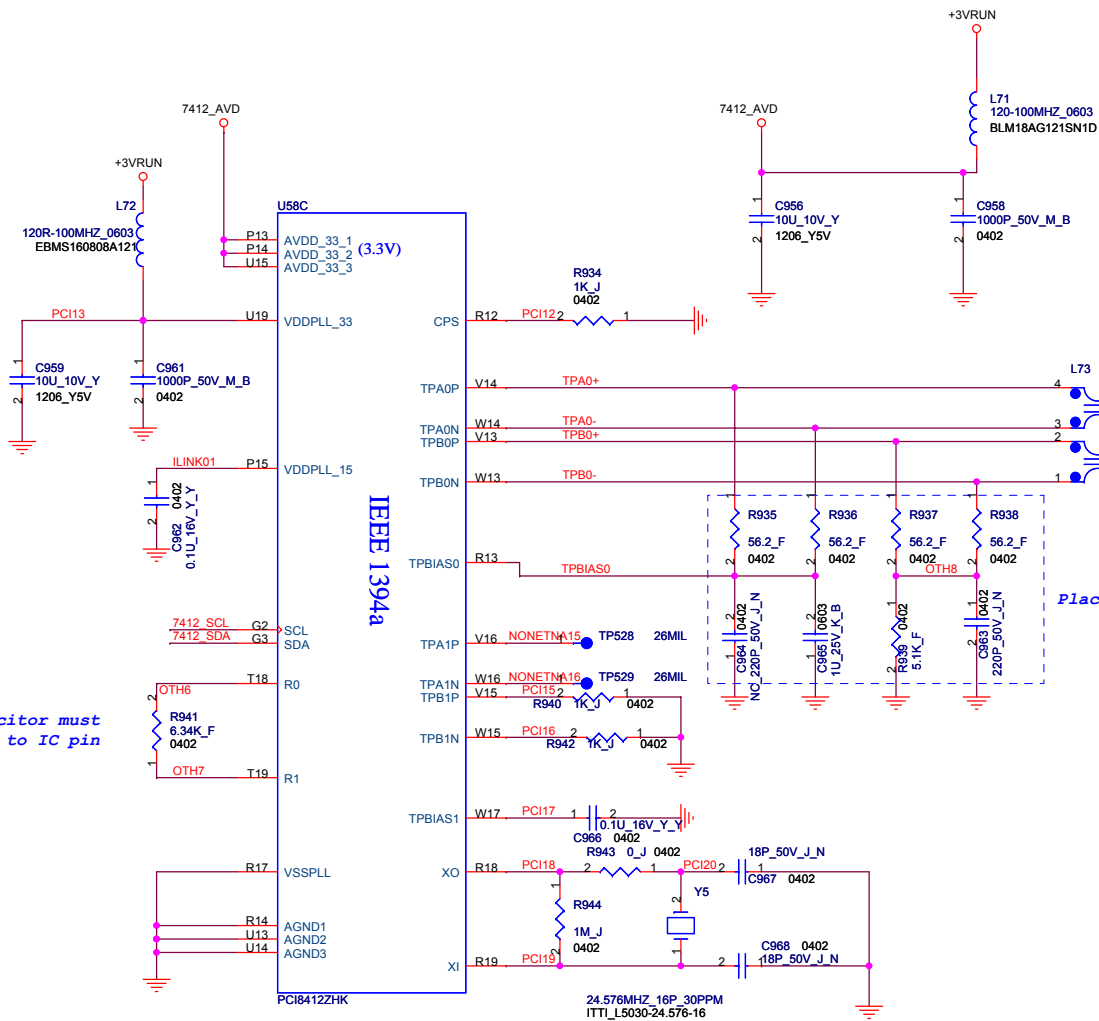






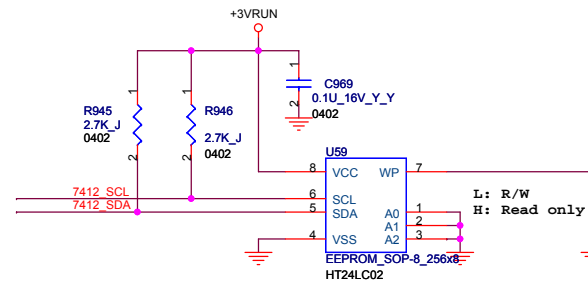


This capacitor must be placed to IC pin

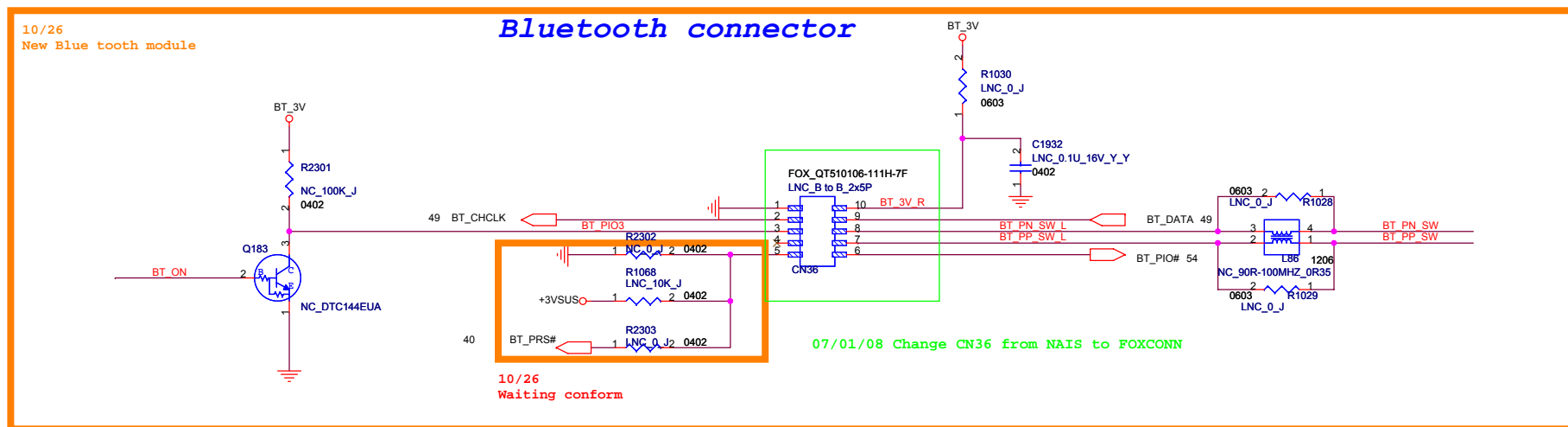
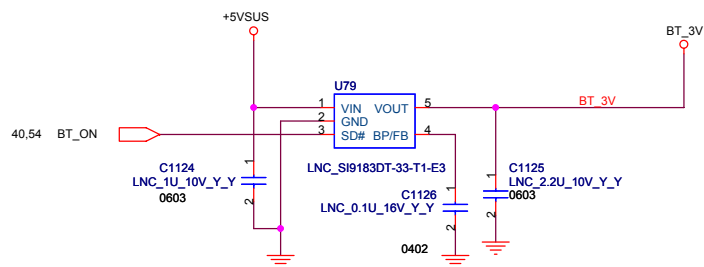


iLink CONN.

Place near PCI7412.



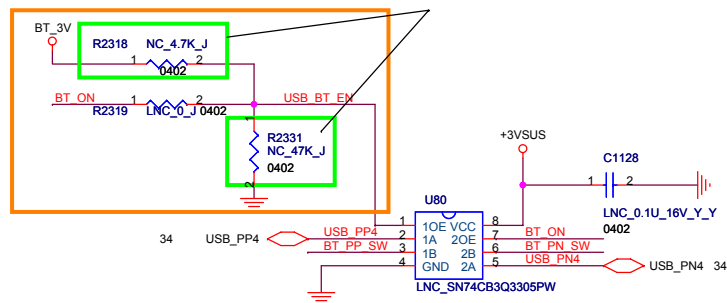
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
PCI (iLINK)			
Size	Document Number	Rev	
A3	(HAI)-01 / Main Board (MBX-176) 2007.1.4	2.0	
Date:	Primary: October 19, 2007	Sheet	45 of 77



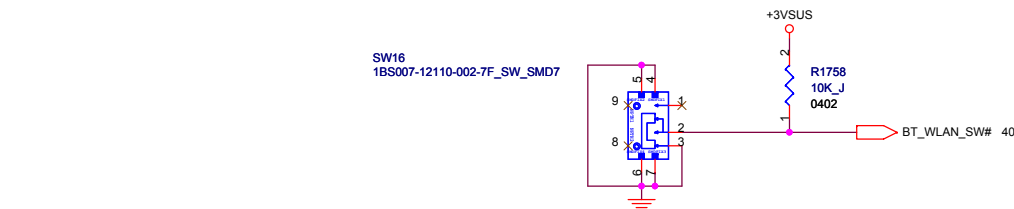
11/04 Change U80 Enable from BT_ON to BT_3V
U79 LDO Ton Max is 1000us
U80 BUS Switch Ton Max is 5ns

12/27 Change Bluetooth circuit Value to LNC_* for M610 DVT I SKU

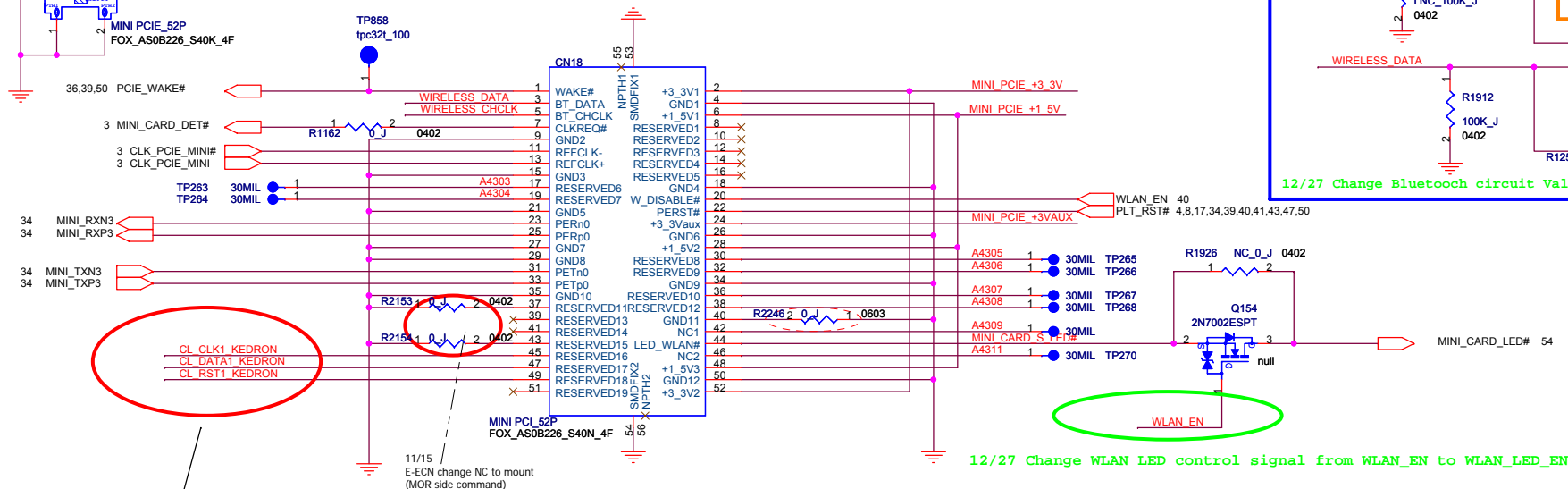
12/14 Change R2318 from 1K to 4.7K, Add one 47K pull up resistance



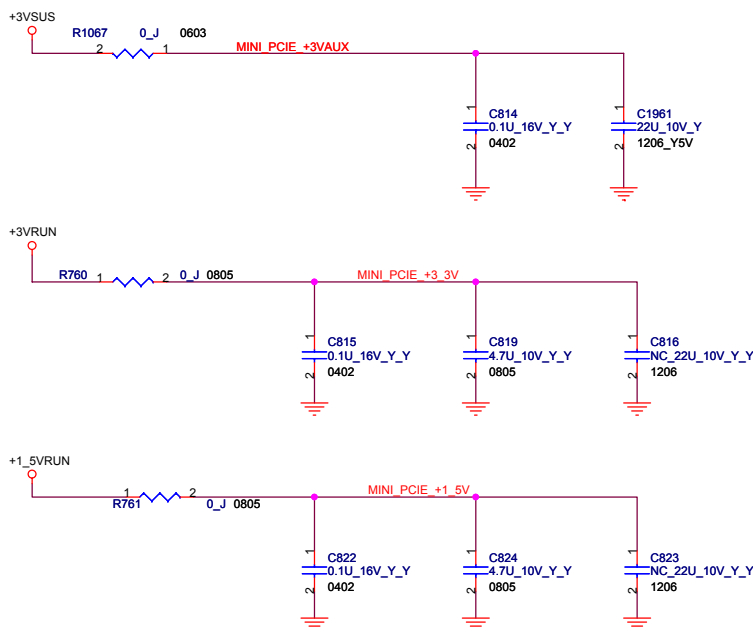
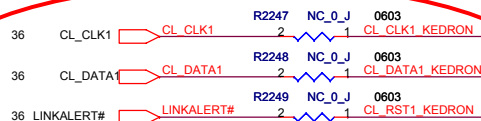
To solve U80 enable pin (net name USB_BT_EN) floating during U79 (BT_3V from LDO)BT_ON desable,
Add Pull low 47K(R2331) at net USB_BT_EN, Change R2318 from 10K to 1K.

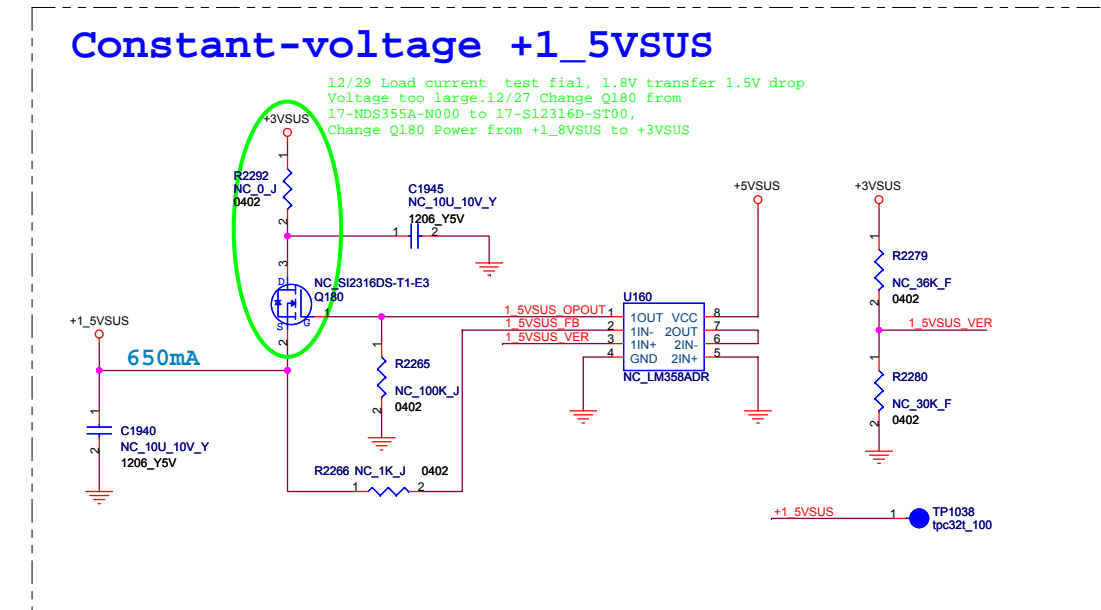
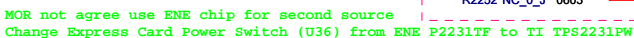


Mini-PCIE Card connector



10/27 FAE suggest
CL_CLK1/CL_DATA1/CL_RST1 can be left as NC if unused iAMT. Don't need to connect to WLAN card.



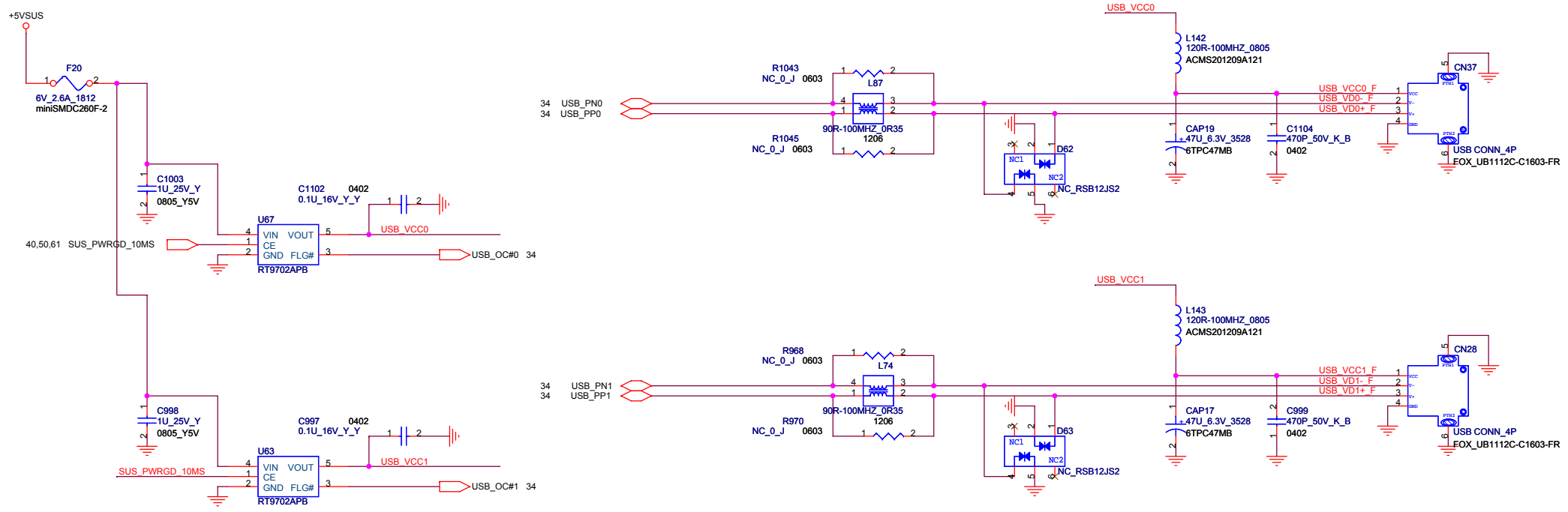


2

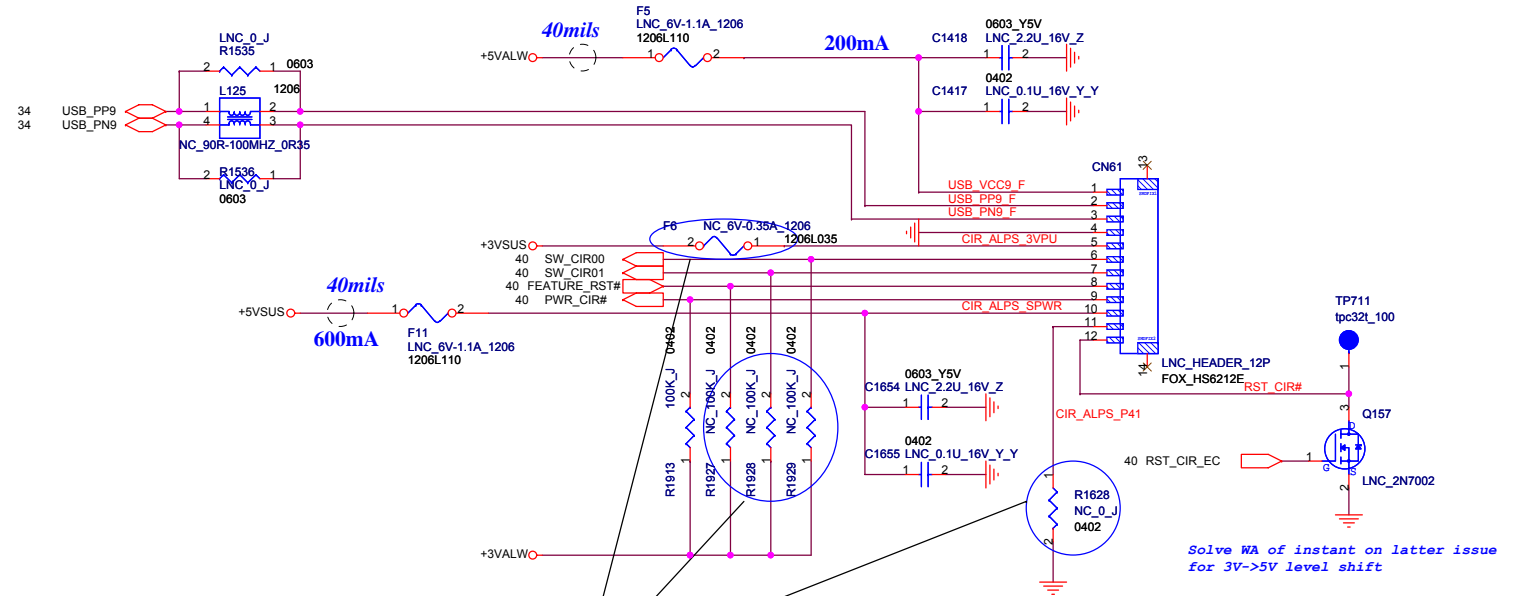


1

USB connector *2



IR Rreceiver connector



Button		SW1	SW0
VAIO button	Kick Instant On	L	L
Green button	Kick Windows	L	H
Shortcut button	Kick Windows	H	L
Standby button	Kick Windows	H	H

Num	Signal Name	I/O	Comment	Difference from ALPS.
1	+5VALW	VCC		<-
2	USB+	I/O		<-
3	USB-	I/O		<-
4	GND	GND		<-
5	+3VSUS	-	Not for use. Because SMK's IC use internal pull up resistor for D-.	ALPS's IC use this signal as a pull up plane of D- for low speed detection.
6	SW0	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
7	SW1	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
8	Feature RST#	I	Software reset signal. (3.3V internal pull up resistor.)	Use for detecting of the remote button. 3.3V open drain output.
9	PWR#	O	Power on request signal. Open drain output.	<-
10	SPWR	I	Power OK signal. 5V input.	<-
11	EN	-	Not for use.	Low: Disable instant on feature Open or High: Enable instant on feature (3.3V internal pull up resistor.)
12	Hard RST#	I	Hardware reset.	<-

9/26 FOR NEW SMK IR module compatiy
1.Change stuff to NC:F6,R1927,R1928,R1929,
2.EC Page GPIO20(105),GPIO2(83) pin swape

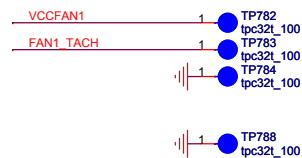
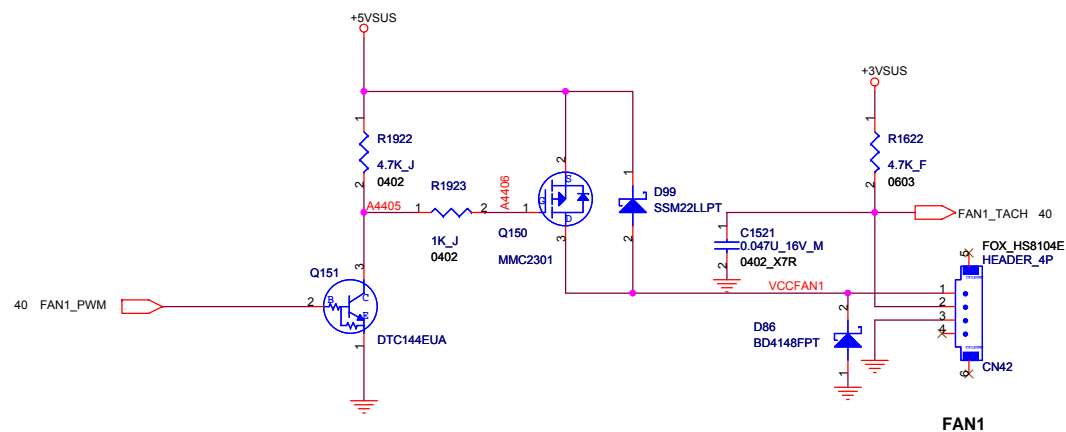
12/27 Change CIR circuit Value to LNC_* for M610 DVT L SKU

At Only USB Internal CIR, it's USB Power

USB_VCC9_F	1	TP847
USB_PP9_F	1	TP848
USB_PN9_F	1	TP849
	1	TP850
CIR_ALPS_3VPU	1	TP851
SW_CIR00	1	TP852
SW_CIR01	1	TP853
FEATURE_RST#	1	TP854
PWR_CIR#	1	TP855
CIR_ALPS_SPWR	1	TP856
	1	TP857

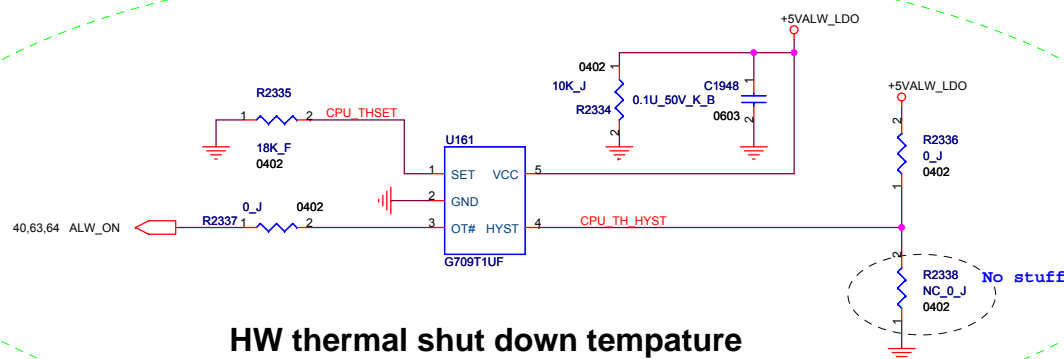
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		LED/LID SW#/Touch PAD	
Size	Document Number	Date	Rev
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	Friday, October 19, 2007	2.0
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FAN circuit



HW THERMAL PROTECTION

07/01/09 Change HW THERMAL PROTECTION circuit to stuff

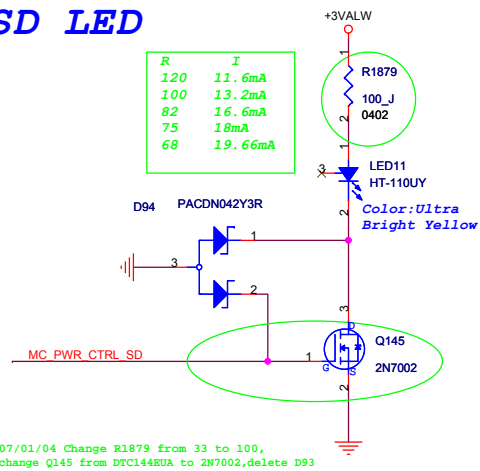


**HW thermal shut down tempature
setting 95 degree . Put Near CPU .**

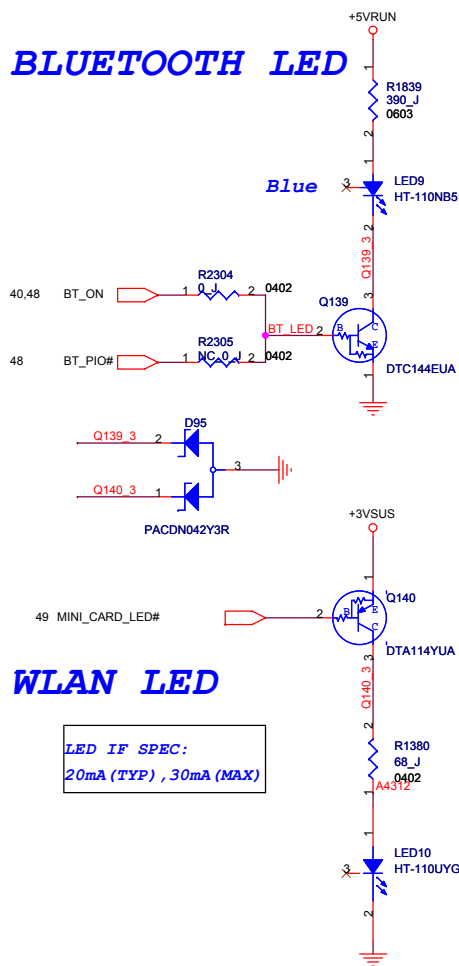
Base on MOR side request to add HW thermal protection circuit

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
Size		Document Number	
43		(M610-1-01) MainBoard (MBX-176) 2007/4/9	
Date:		Rev	
Friday, October 19, 2007		Sheet 53 of 77	

SD LED



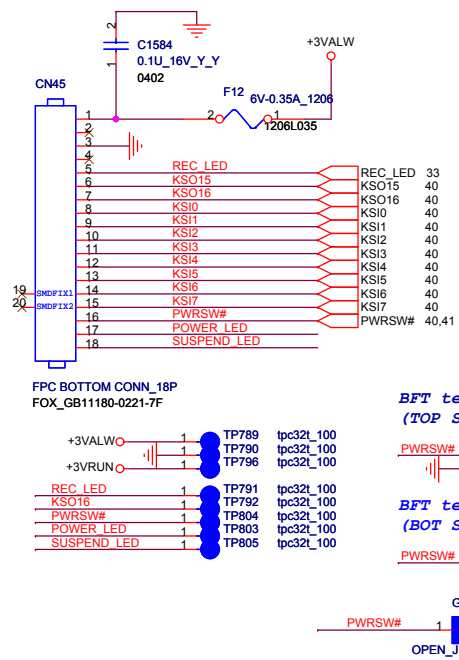
BLUETOOTH LED



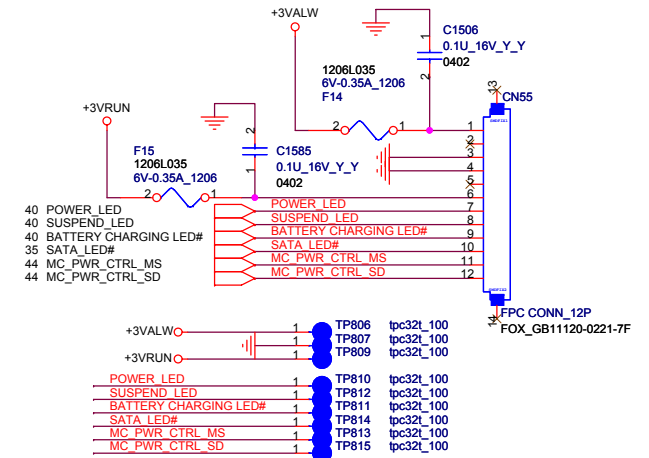
WLAN LED

LED IF SPEC:
20mA (TYP) , 30mA (MAX)

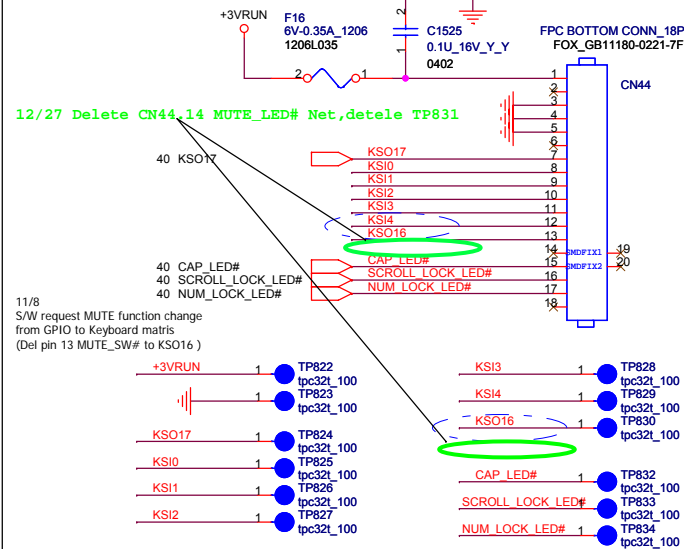
To Power Button Board Connector



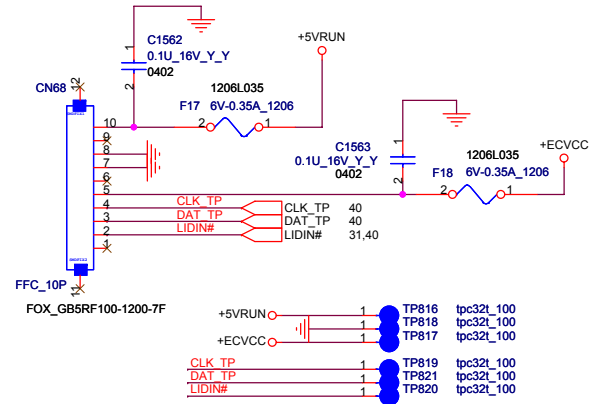
To LED Board Connector



To AV Function Board Connector



To Touch Pad Board Connector



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

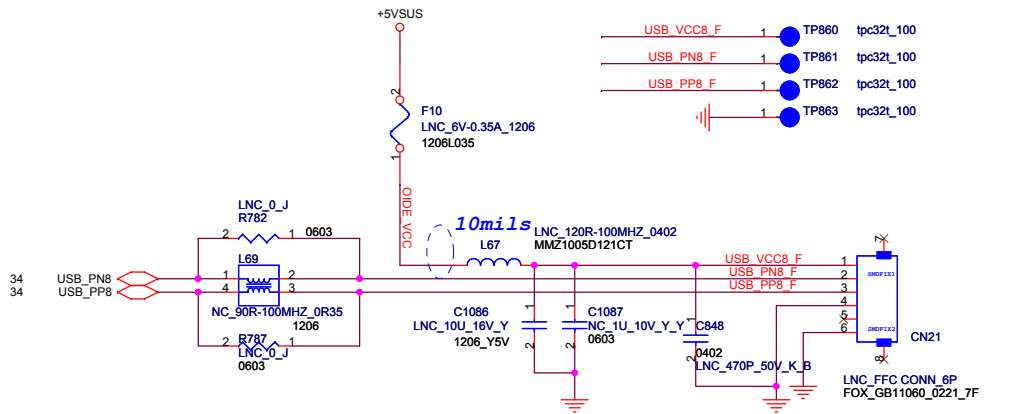
Title POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED

Size Document Number

43 (M610-1-01) MainBoard (MBX-176) 2007.1.4

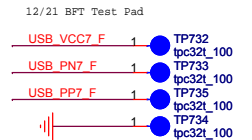
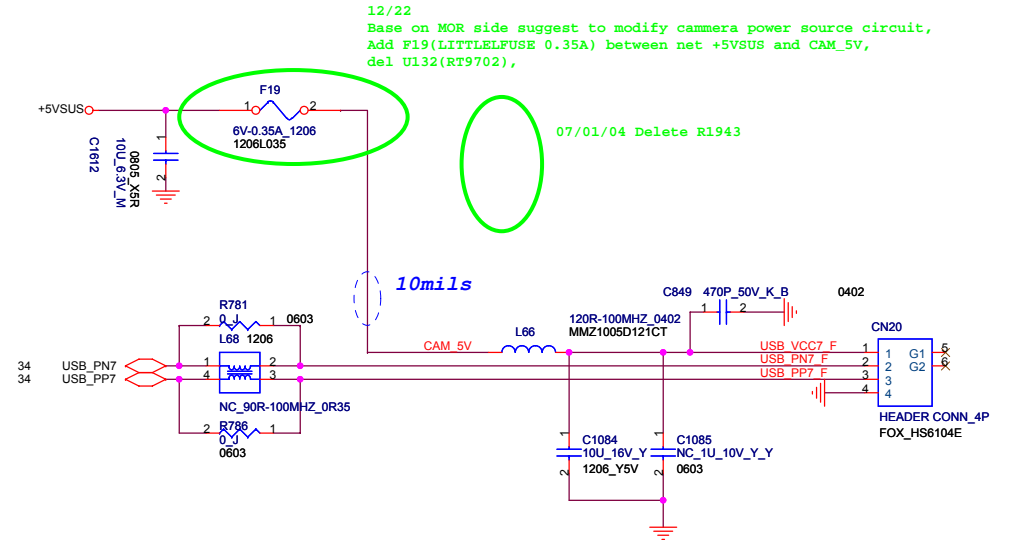
Date: Friday, October 19, 2007 Sheet 54 of 77

OIDE Connector

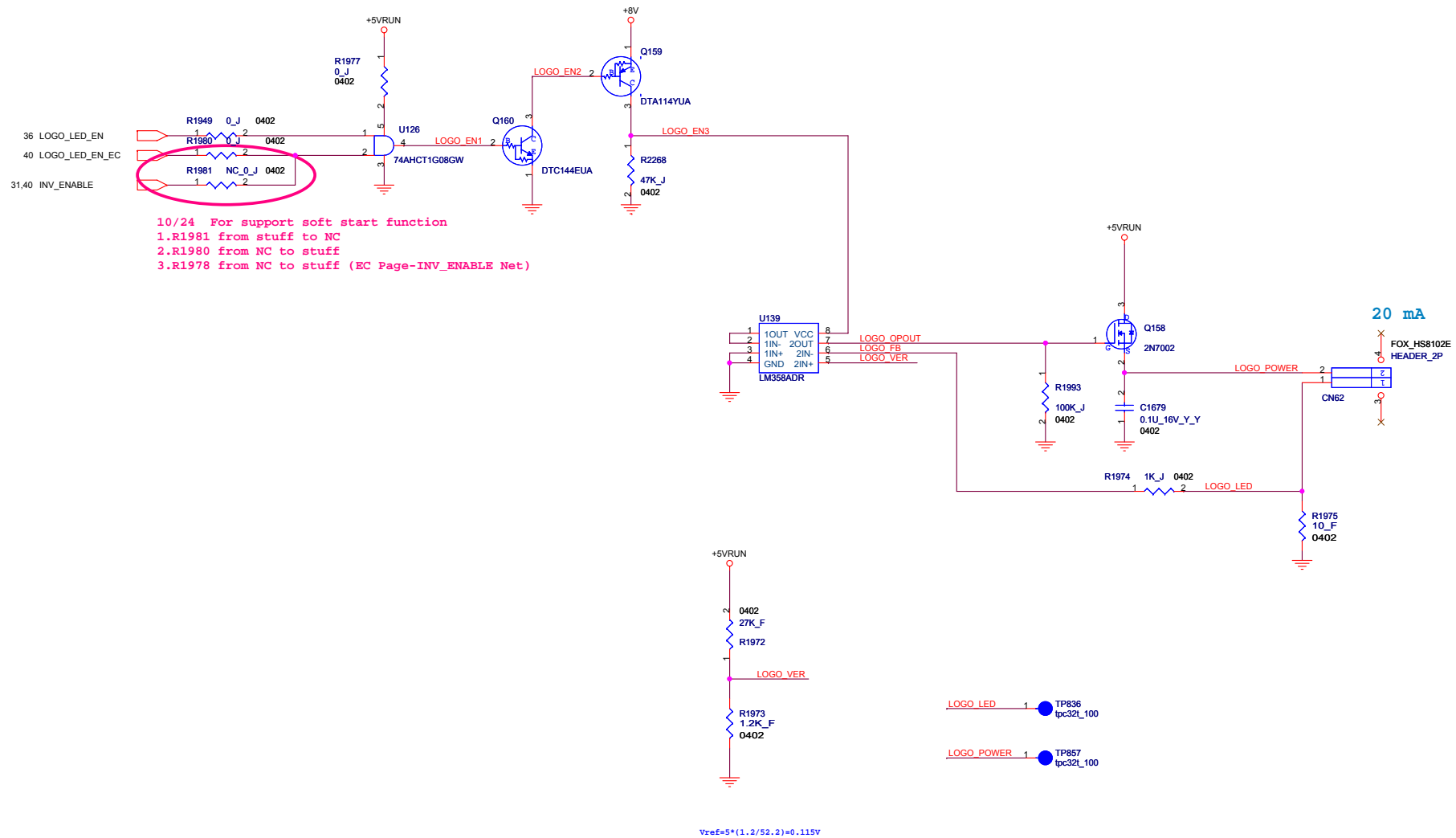


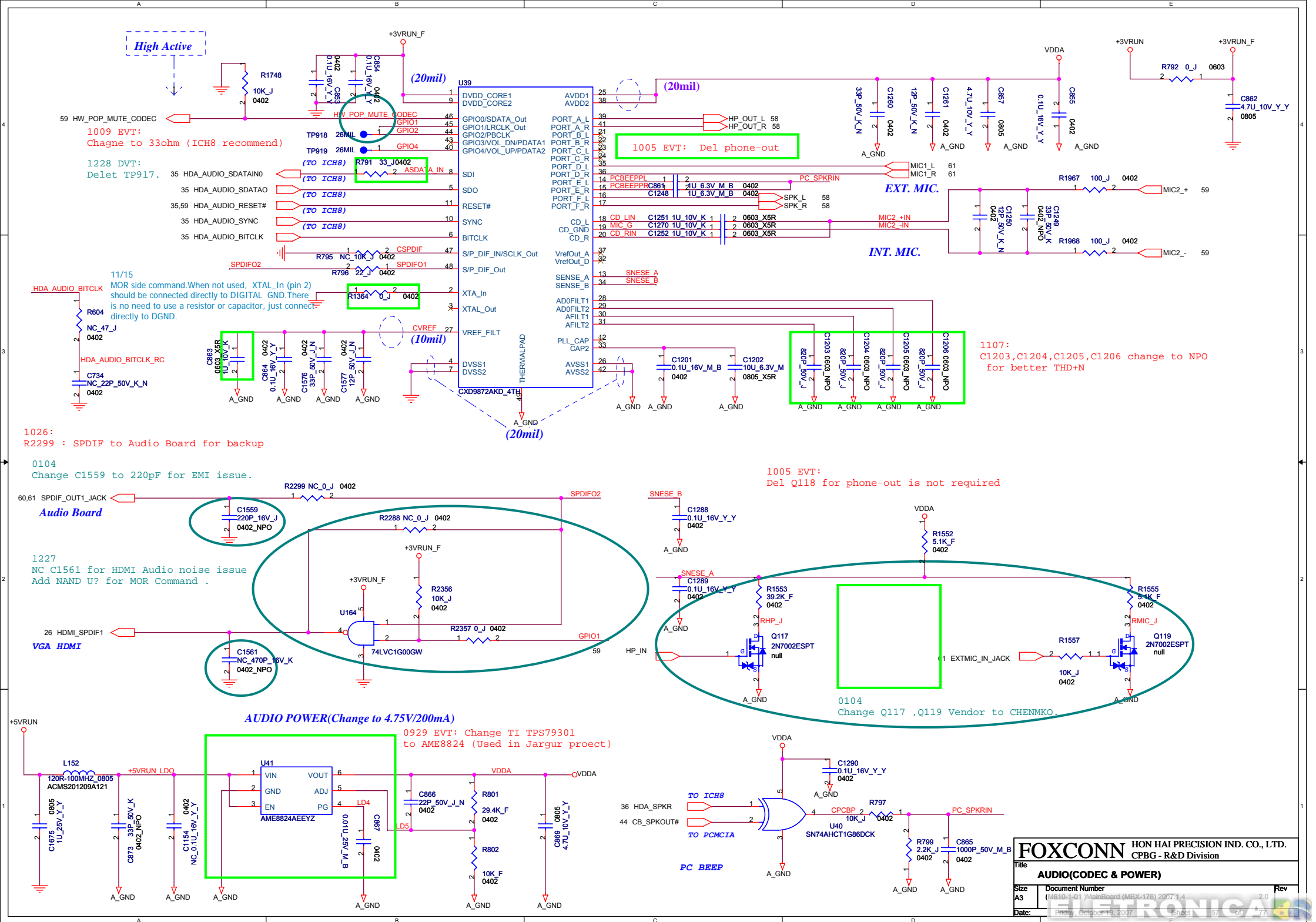
12/27 Change Felica circuit Value to LNC_* for M610 DVT L SKU

CAMERA Connector

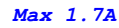


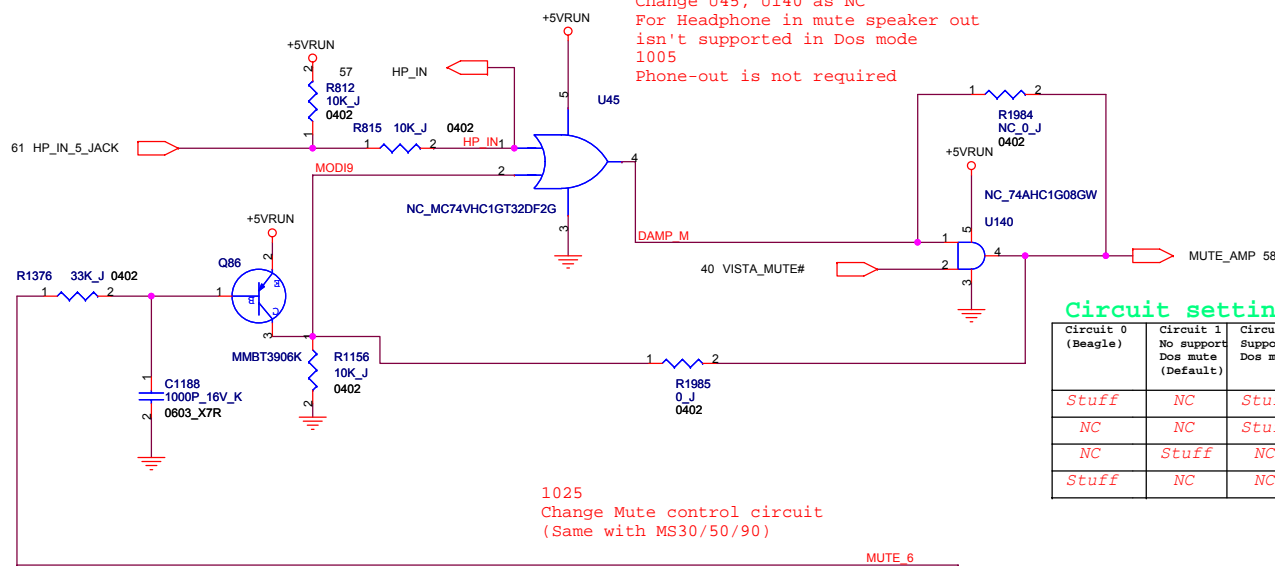
Constant-Current SONY LOGO LED





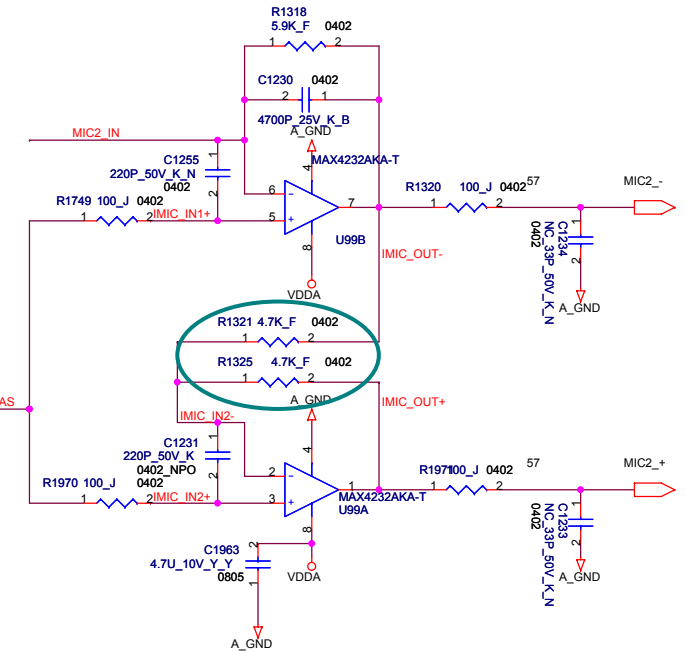
1228 Change CAP39 and CAP40 Vendor from LELON to Panasonic





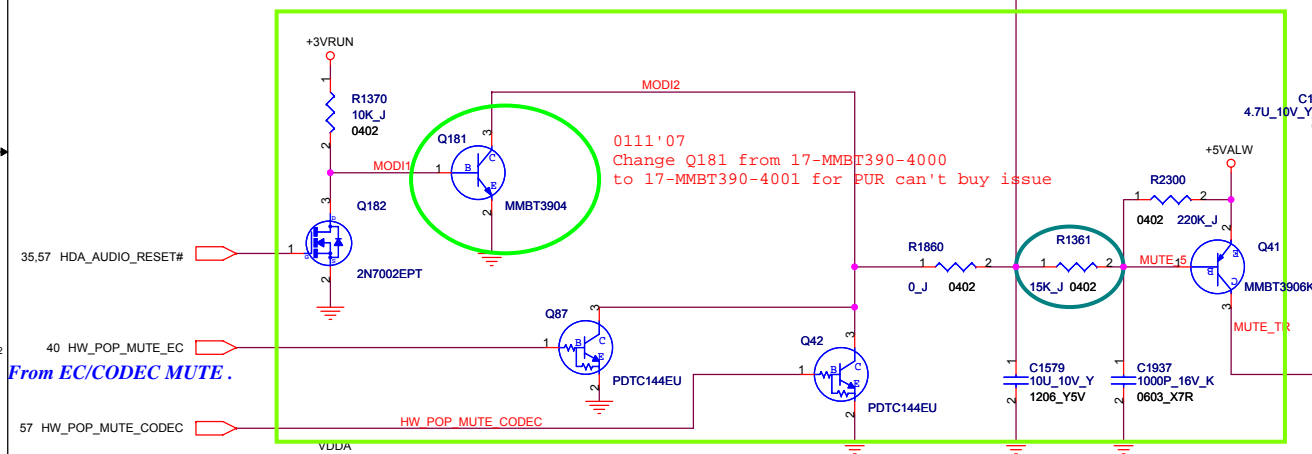
Circuit setting table

Circuit 0 (Beagle)	Circuit 1 No support Dos mute (Default)	Circuit 2 Support Dos mute	component
Stuff	NC	Stuff	U45
NC	NC	Stuff	U140
NC	Stuff	NC	R1985
Stuff	NC	NC	R1984



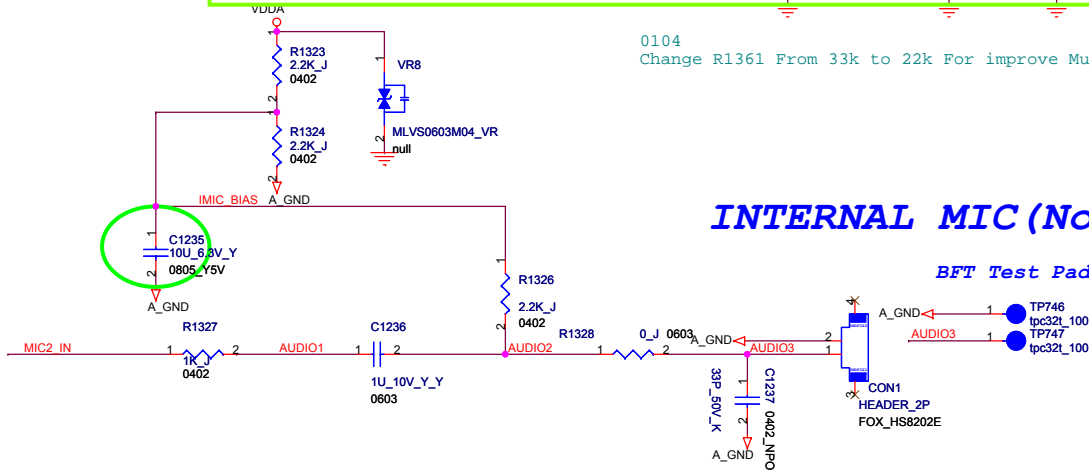
1227
Change R1321 and R1325 from 4.7k_J to 4.7K_F
for MOR Side Command.

1005
Del phone-out mute circuit
for phone-out is not required

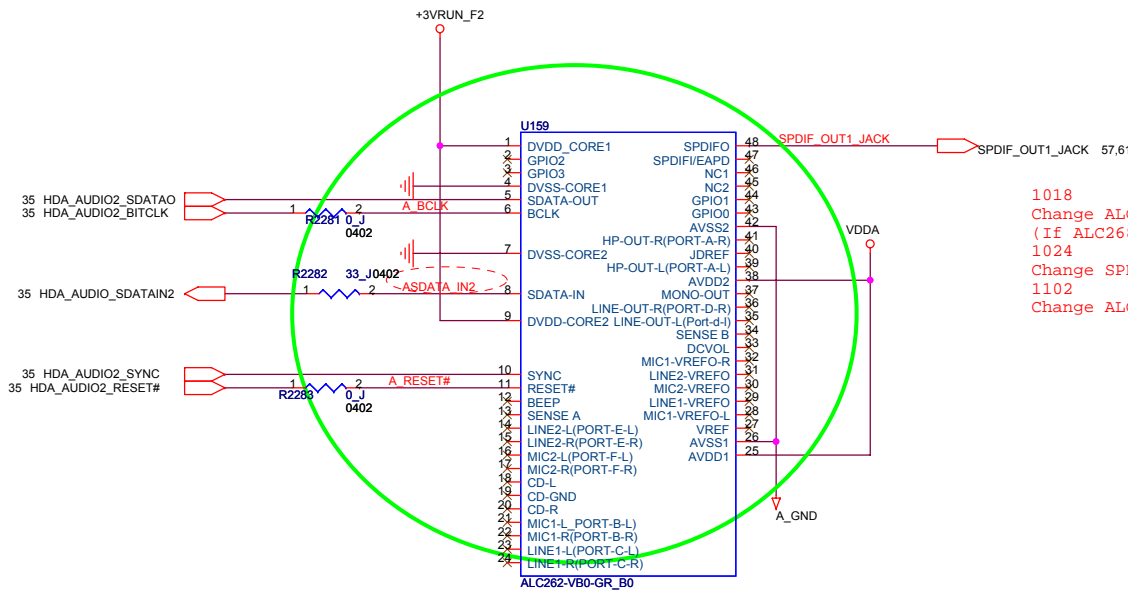
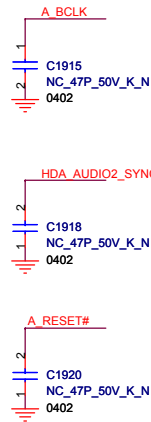


0104
Change R1361 From 33k to 22k For improve Mute_TR signal quality well.

INTERNAL MIC (Non)

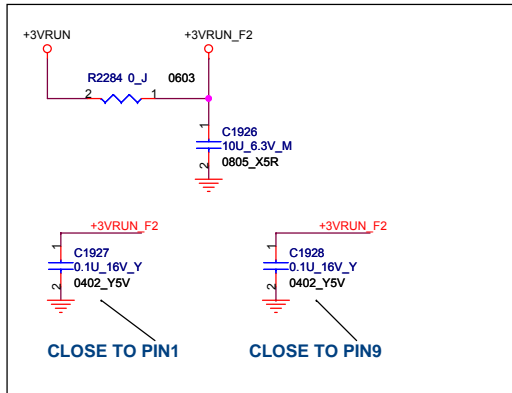


Anti-Glitch

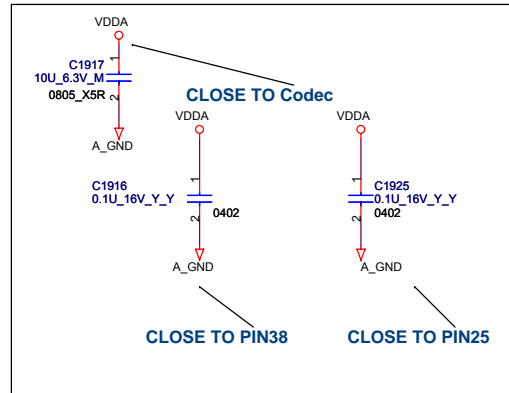


1018
Change ALC262 to ALC268.
(If ALC268 sample schedule delay, change to ALC262)
1024
Change SPDIF of Second codec to MB optical out
1102
Change ALC268 to ACL262

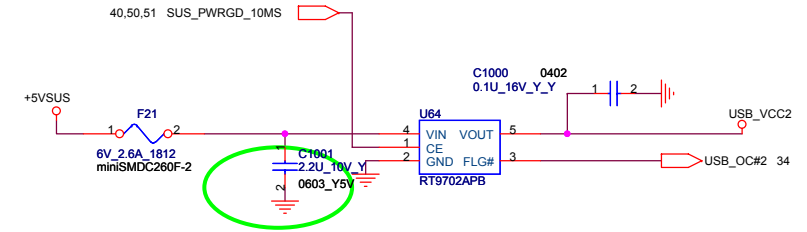
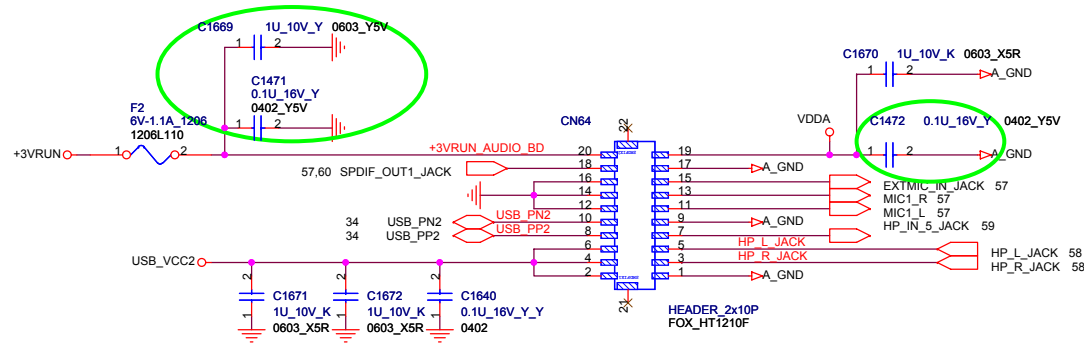
Decoupling Caps, place close to power pin.



Decoupling Caps, place close to power pin.

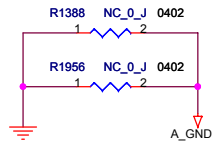


Audio Board connector

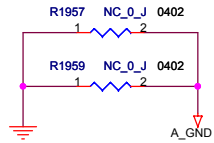


Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

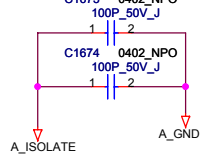


Close screw hole H5

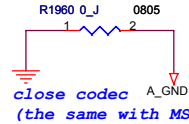
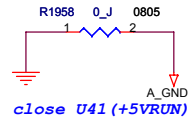
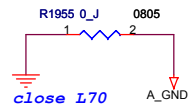


Isolate screw hole H4, and add EMI/ESD solution

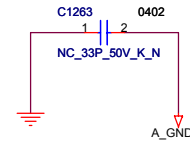
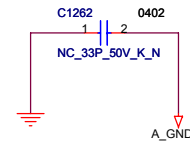
EMI



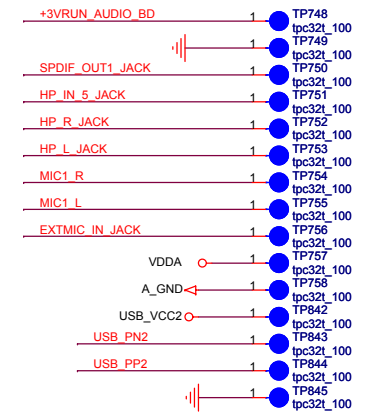
Add jumper resistor for Return patch

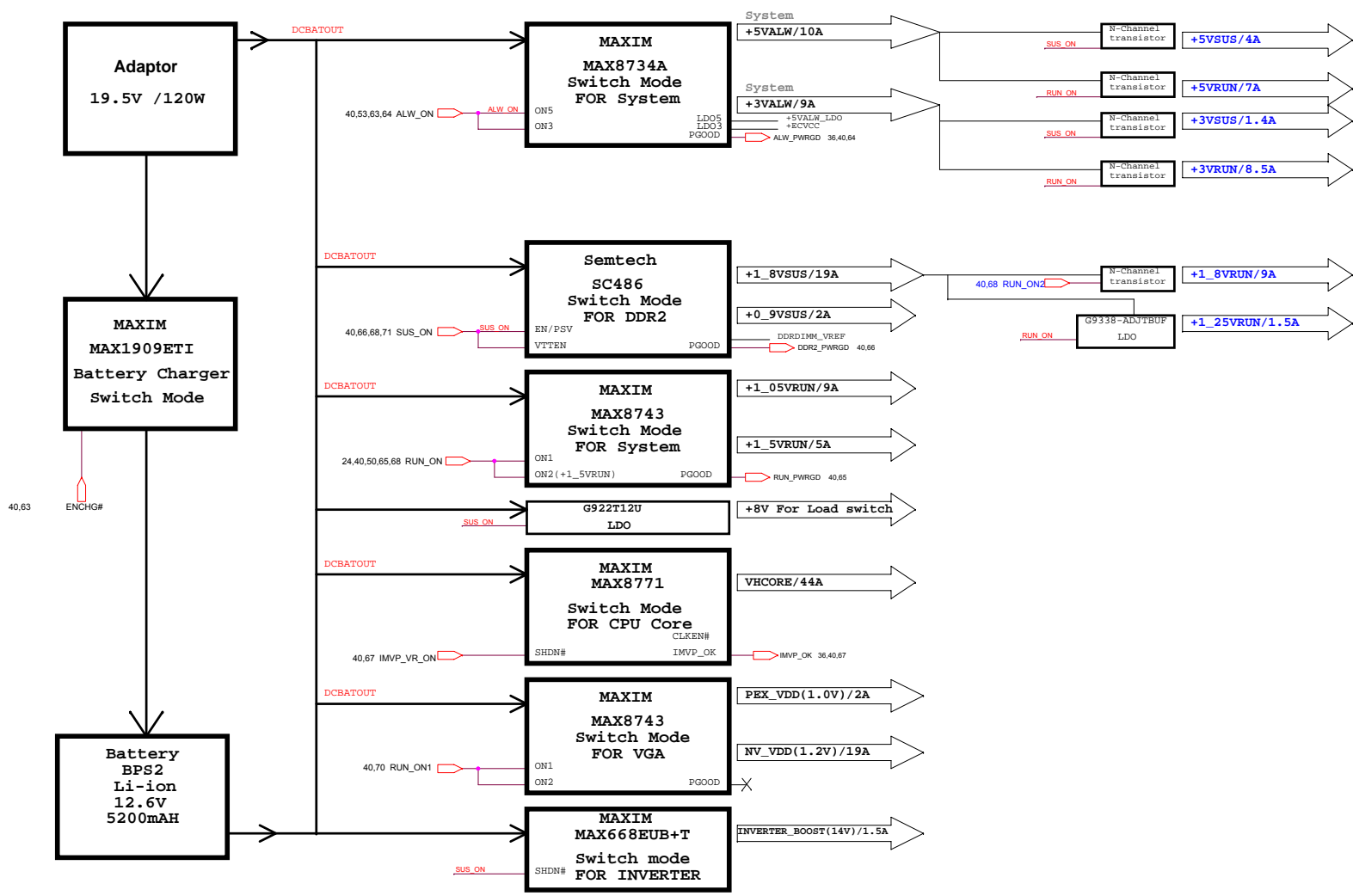


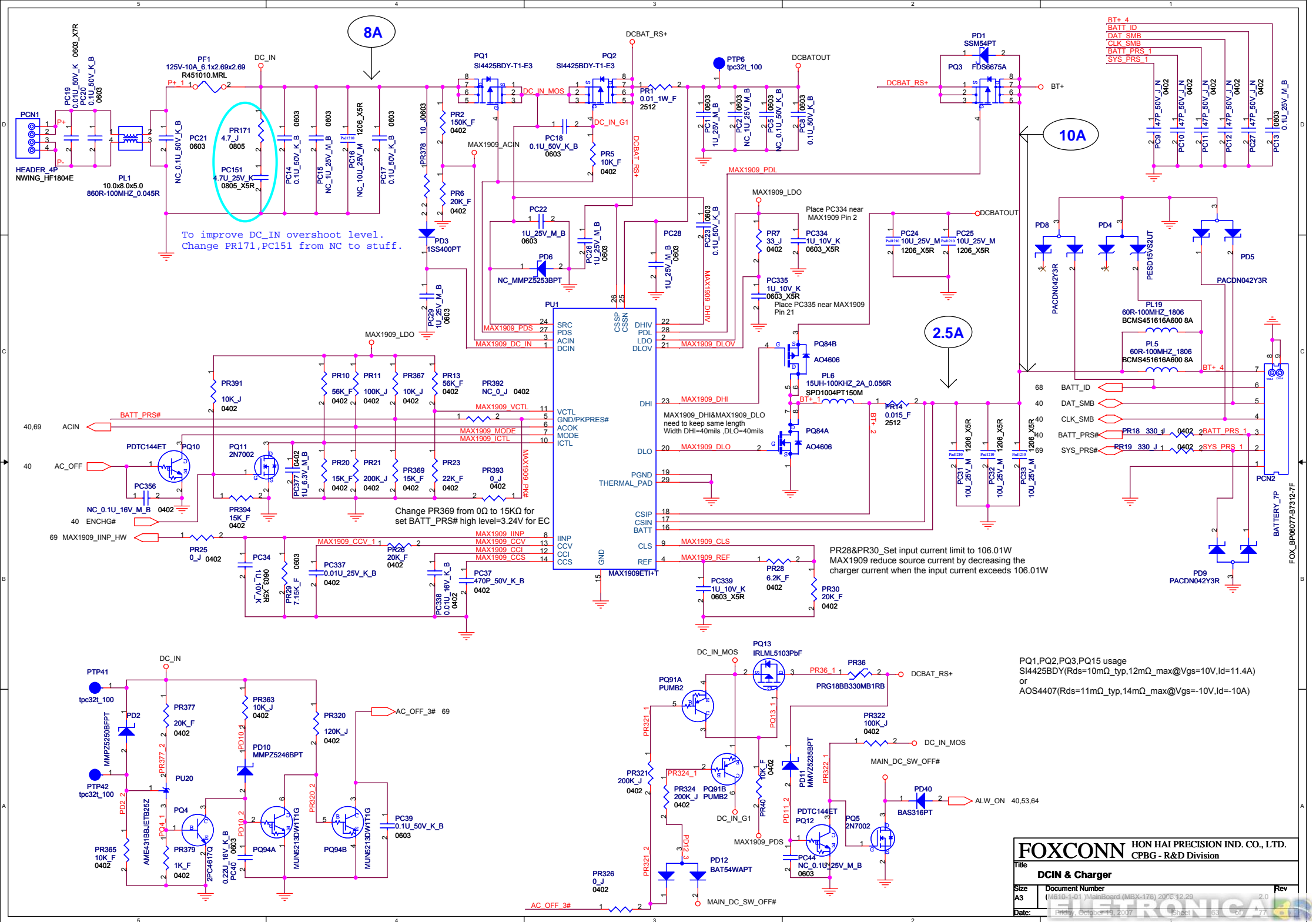
Original EMI back up solution to continue with MS20 (bridge between GND and A_GND)

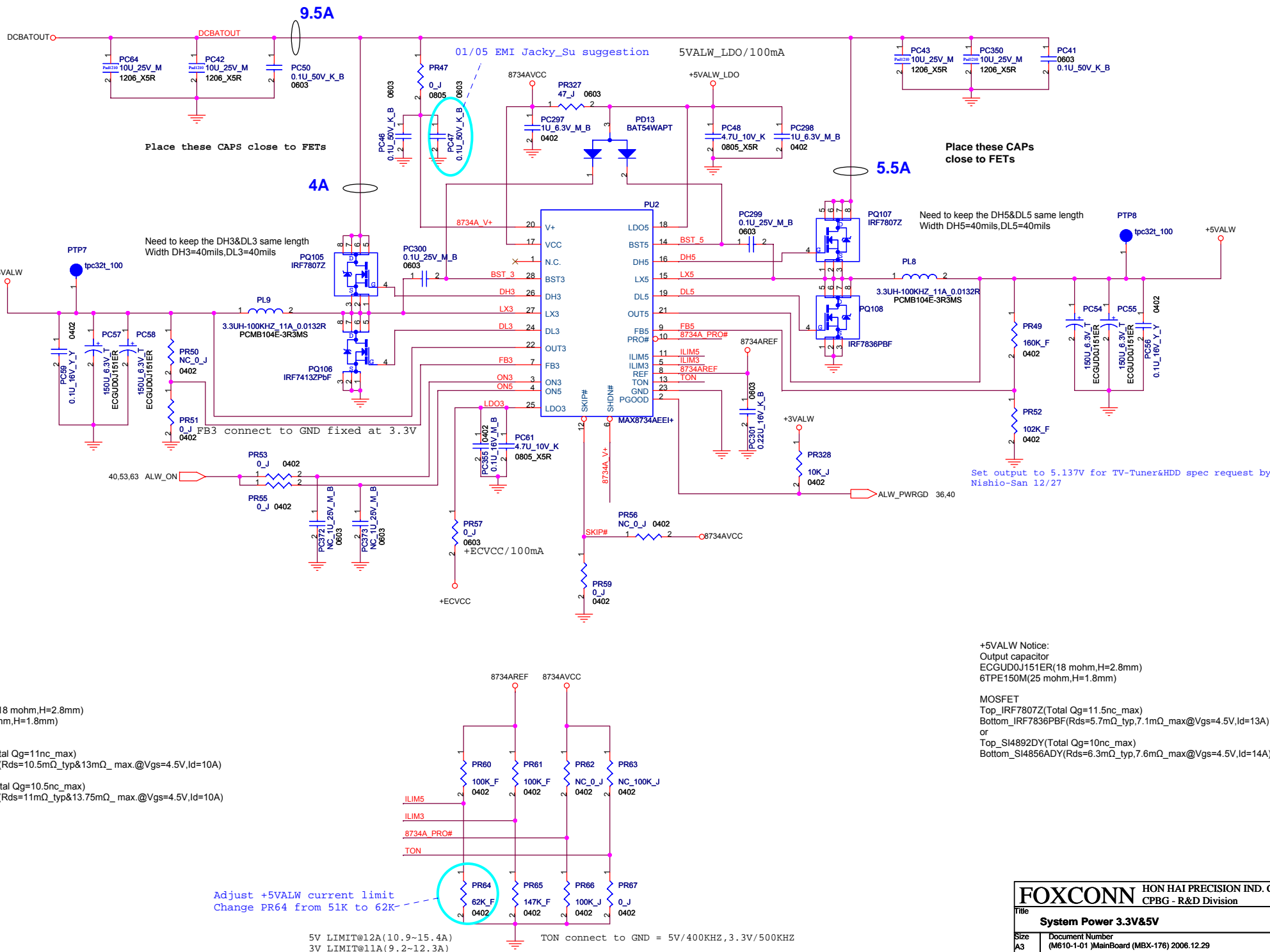


BFT Test Pad

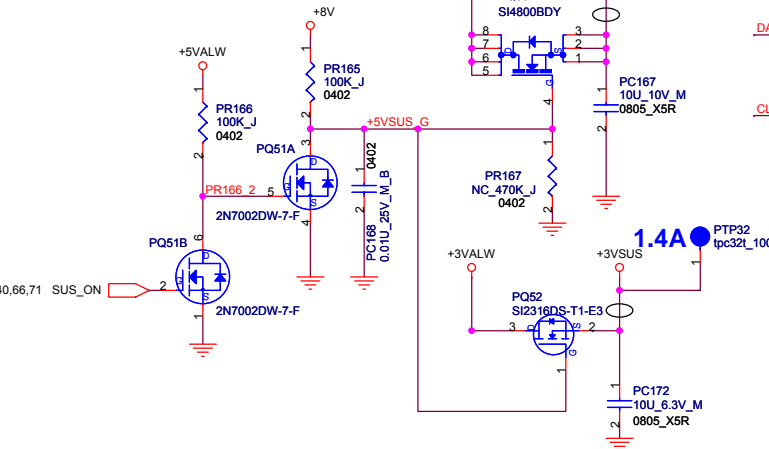




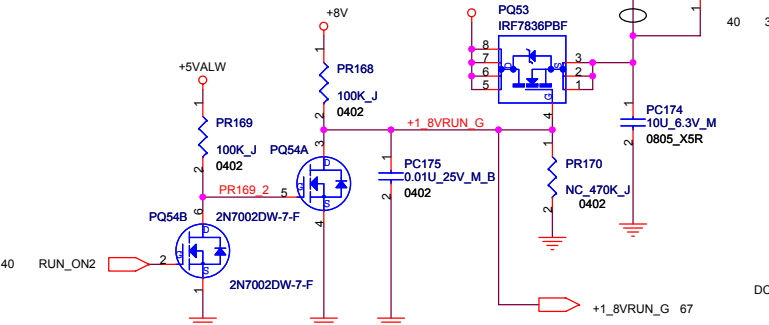




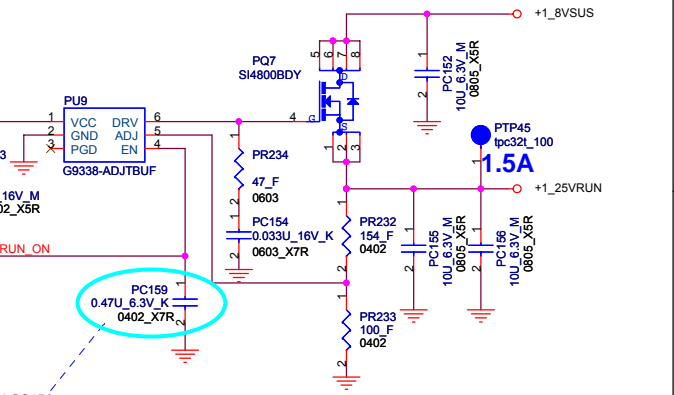
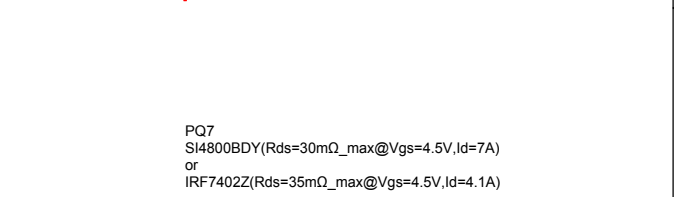
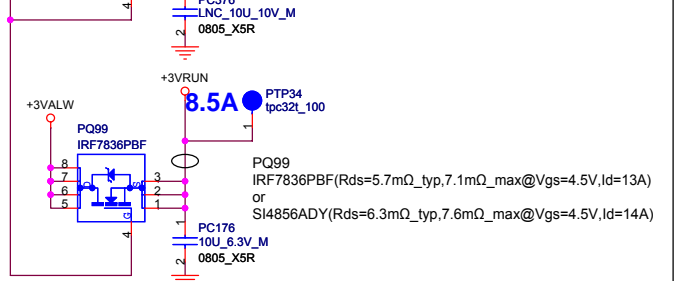
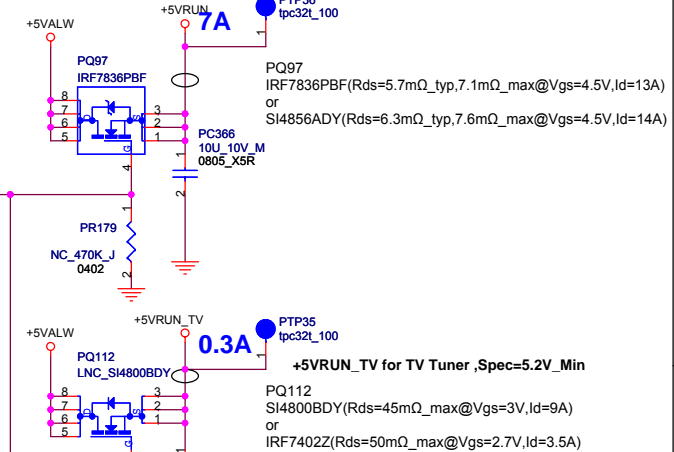
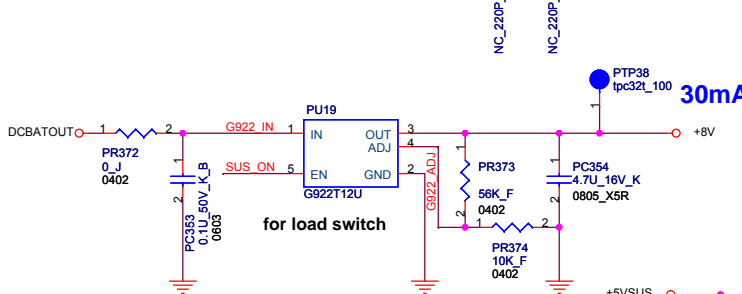
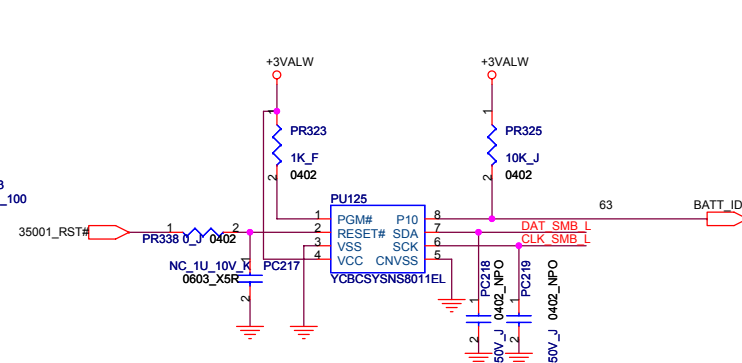
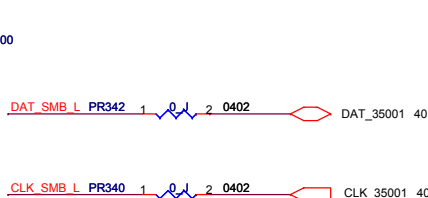
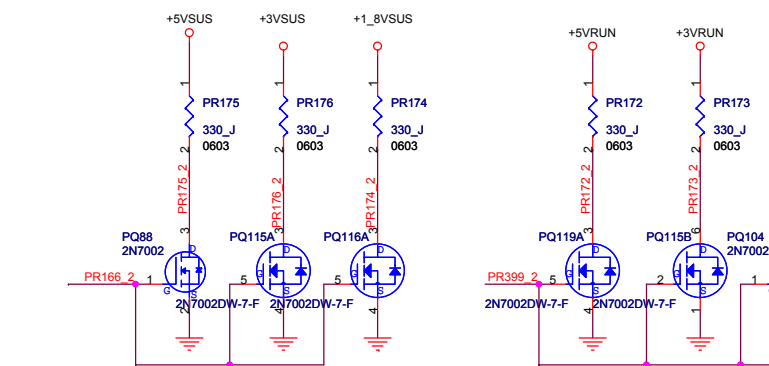
PQ50
SI4800BDY(Rds=45mΩ_max@Vgs=3V,Id=9A)
or
IRF7402Z(Rds=50mΩ_max@Vgs=2.7V,Id=3.5A)



PQ53
IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

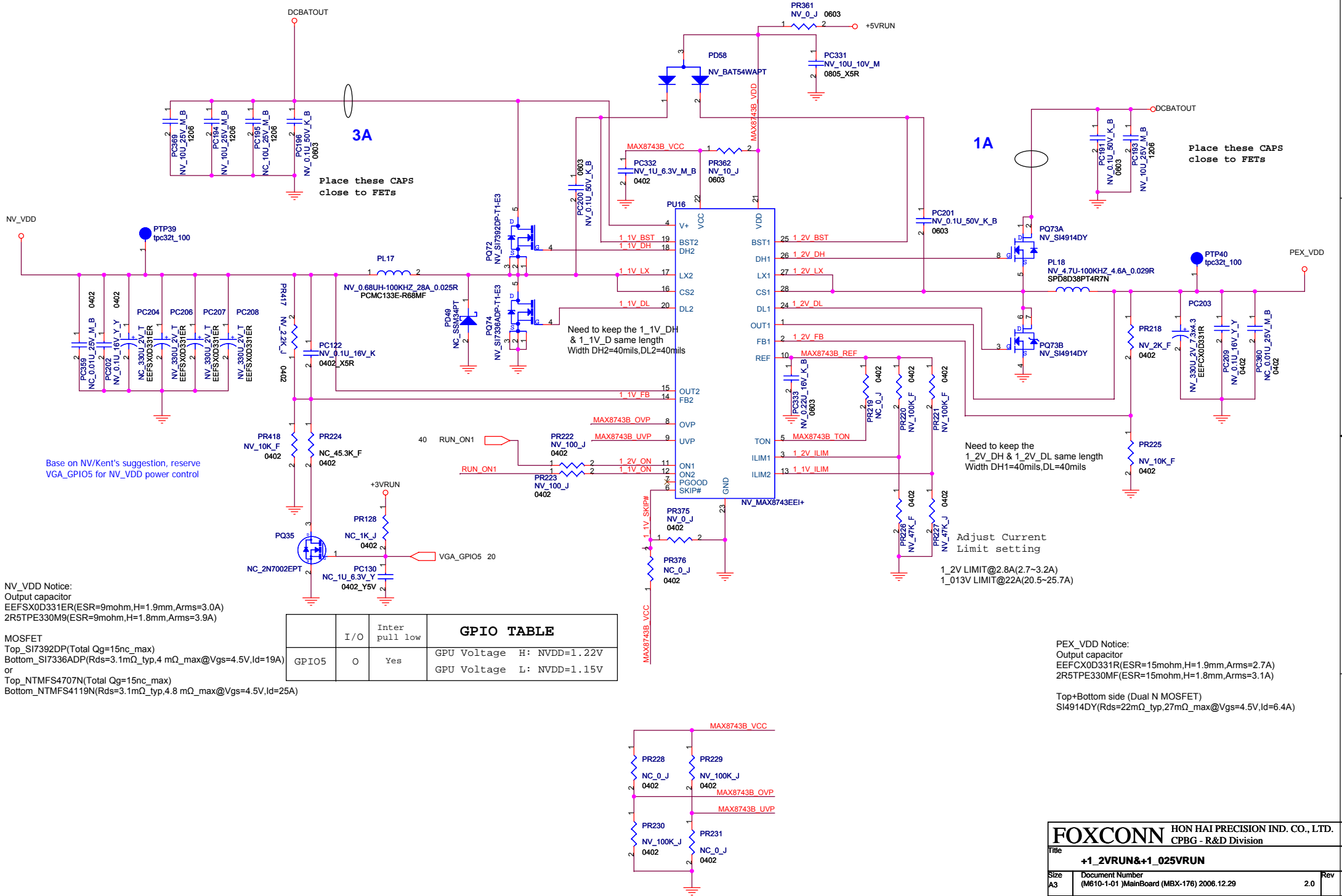


Discharge circuit for power-off



11/16 PC159
shortage issue
Change X5R (1C-2B20474-M000)
to X7R (1C-2B20474-K000)

FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Other power plan			
Size	Document Number		Rev
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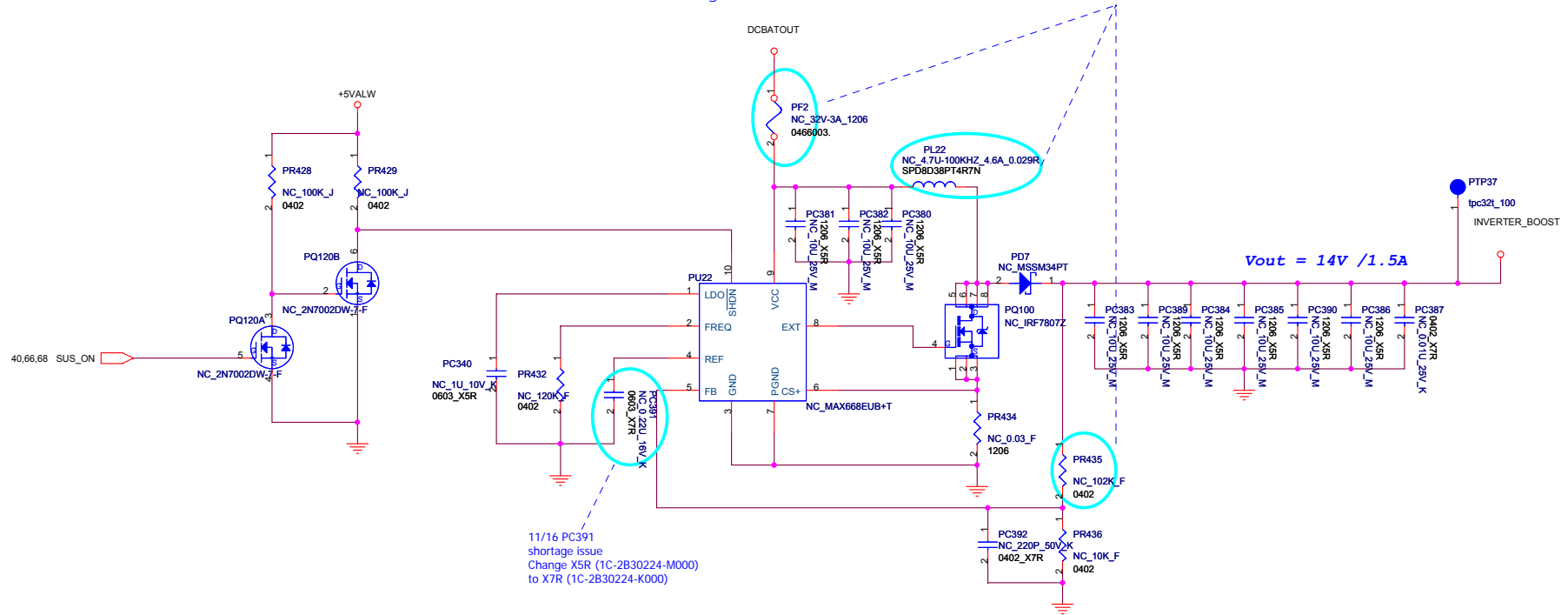


NV_VDD Notice:
Output capacitor
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_Si7336ADP(Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

GPIO TABLE			
	I/O	Inter pull low	
GPIO5	O	Yes	GPU Voltage H: NVDD=1.22V GPU Voltage L: NVDD=1.15V

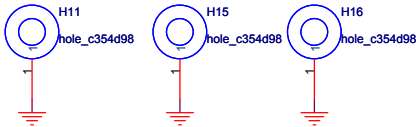
PEX_VDD Notice:
Output capacitor
EEFCX0D331R(ESR=15mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)
Top+Bottom side (Dual N MOSFET)
SI4914DY(Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)

Boost circuit design change.
 Add PF2 (32V-3A_1206) fuse for boost circuit,
 Change PL22 from 8UH-100KHZ_2.5A_0.07R to 4.7U-100KHZ_4.6A_0.029R.
 Change PR435 from 95.3K to 102K



HOLE

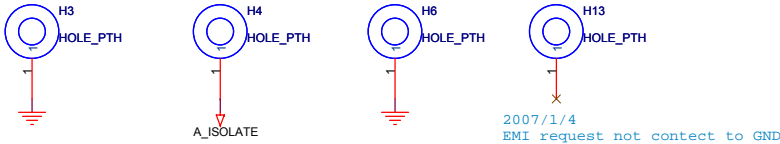
Type 1



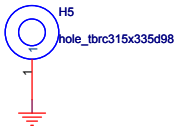
Type 2

Type 3

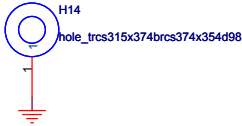
Type 4



Type 5



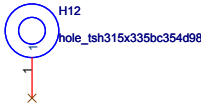
Type 6



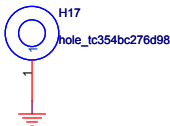
Type 7



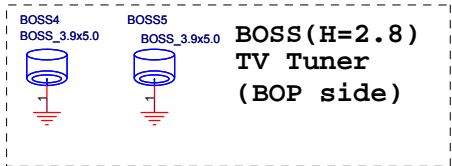
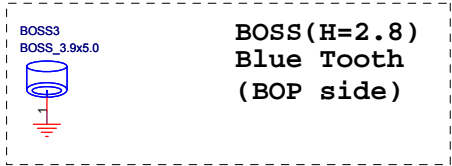
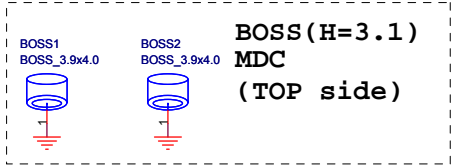
Type 8



Type 9



Type CPU



Type NPPTH Guide (spherical)HOLD



Type NPPTH Guide (oval-shaped)HOLD



M612 DVT1 Change Circuit

1. (Page 4) 07/08/29 For support Penryn-CPU, change U2-CPU Thermal Senser from GMT to SMSC.
2. (Page 44) 07/08/29 Change System ID to M612 Type
3. (Page 69) 07/10/19 Add C1966-0.1u to PD54-pin2 for UL-LUCK issue

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
History(EVT to MP)			
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A3	(M810-1-01) MainBoard (MBX-176) 2007.1.4		5
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